Temperature-Aware Design and Management for 3D Multi-Core Architectures

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Abstract

Vertically-integrated 3D multiprocessors systems-on-chip (3D MPSoCs) provide the means to continue integrating more functionality within a unit area while enhancing manufacturing yields and runtime performance. However, 3D MPSoCs incur amplified thermal challenges that undermine the corresponding reliability. To address these issues, several advanced cooling technologies, alongside temperature-aware design-time optimizations and run-time management schemes have been proposed. In this monograph, we provide an overall survey on the recent advances in temperature-aware 3D MPSoC considerations. We explore the recent advanced cooling strategies, thermal modeling frameworks, design-time optimizations and run-time thermal management schemes that are primarily targeted for 3D MPSoCs. Our aim of proposing this survey is to provide a global perspective, highlighting the advancements and drawbacks on the recent state-of-the-art.

Keywords: System-Level Design, Thermal Management, MPSoC Cooling, Temperature Optimization, Reliability, Vertical Integration.

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1

Introduction

The last decades have seen a revolution in data gathering, processing, information storage and communication. This revolution has been caused by electronic computing systems, which nowadays are one of the key building blocks of the world's information technology (IT) infrastructure. In fact, computing systems and IT services are an essential pillar of the developed world, contributing up to 50% of its economy [1]. The IT and computing systems revolutions have been the result of the advancements in IC processing technology, where the number of components (transistors) on the same die area have been doubled every 18 months [2], which is also known as Moore's law. This has been the drive to generate more complicated computing systems with higher performance and computational functionality.

As feature sizes scale with advanced processing technologies, the performance of processing units has increased because of greater functionality and higher computational capabilities. This functionality augmentation was accompanied by an increase in the operating frequency of the processing unit. Micro-architects have conventionally used operating frequency as a measure for the processing unit performance, as higher frequency implies more instructions executed per unit time.

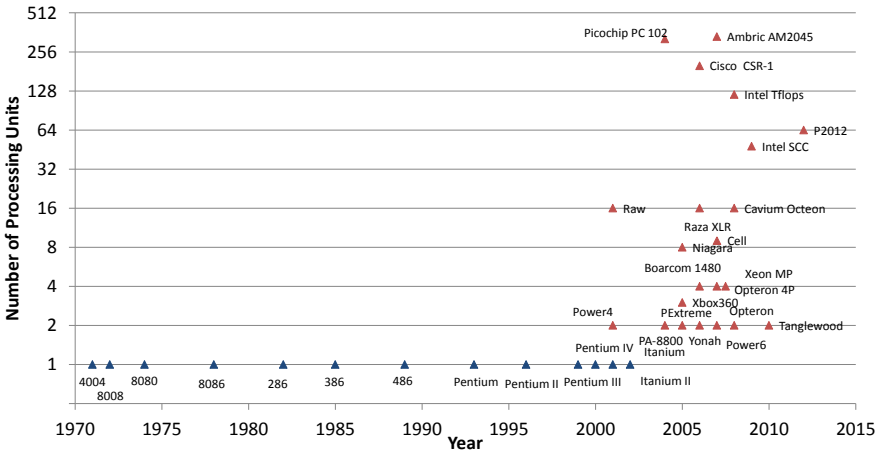


Figure 1.1: Number of processing units integrated in a single IC, as evolved with time. Blue-labeled ICs are single-core architectures, while red-labeled ICs are multi-core architectures.

However, at the sub-micron level, the circuit-level delays are getting dominated by wiring and interconnect delays, which led to frequency flattening. If the operating frequency would increase with this technology, significant additional power consumption is required by the processing unit, which results in an increased heat generation. For example, a 90 nm fabricated AMD processing unit would require 60% additional power consumption to increase the operating frequency by 400MHz [3].

Multi-core architectures have been proposed as an alternative design paradigm to frequency increase in single-core architectures, to continue performance improvement with technology scaling [4]. Multi-core architectures integrate two or more processing units, with shared or distributed memory modules, interconnected through an on-chip bus or a network-on-chip [5]. As feature sizes scale with advanced processing technologies, the number of processing units in multi-core architectures dramatically increases. Fig. 1.1[1] shows that the number of cores inte-

[1]This figure is based on a similar figure found in the course slides given by Prof. S. Amarasinghe of MIT http://groups.csail.mit.edu/cag/ps3/pdf/6.189-info-session.pdf

grated in a single IC has started to ramp-up in the beginning of the 21^{st} century. Recent multi-core architectures integrate a number of processing units, multi-level memory hierarchy, an interconnect module, and in the case of embedded domain, special peripherals such as analog-to-digital converters (ADC), co-processors, or wireless RF antennas. This architecture, which is known as *Multiprocessor Systems-on-Chip* (MPSoC), has been widely used in various domains. An example of recent MPSoC utilization at the high performance computing systems level is data-intensive computing systems, which is also known as the *fourth paradigm* [6]. Another example for MPSoC utilization is found at the embedded systems domain, with small- or tiny-size computing systems, such as on-body [7] or in-body [8] health monitoring systems.

1.1 3D-ICs for Augmented Performance Per Unit Area

While the performance of computing architectures has been enhanced by MPSoCs, MPSoCs' performance has been recently challenged by increased propagation delay, primarily due to longer interconnects [9]. This is mainly due to the increased wire-to-gate delay ratio. This delay would lead to degraded MPSoC performance or increased energy consumption.

This delay limitation, combined with the continued demands for increased integrated functionality while preserving the performance and area efficiency, have led to the development of vertically-integrated 3D ICs. 3D integration is viewed as an attractive solution to provide increased functionality with better yield, as well as a technique of combining several technologies in a single enclosure (package) [10]. From a design perspective, 3D integration can be split into the following categories:

- **Monolithic 3D integration** [11]. This integration technology fabricates the tiers serially at the transistor granularity, within a single fabrication process. From the bottom tier, the corresponding transistors are fabricated then a substrate layer is placed on top where another tier is fabricated. These layers are connected with vertical interlayer vias. Thus, this integration technology is

promising in terms of providing higher density and performance gains.

- **3D stacking** (also referred to as Parallel 3D integration) [10]. This integration technology stacks vertically 2D die layers to form a single 3D IC. To enable the communication and power delivery to these dies, there are several techniques adopted such as wire bonding, microbumps, and *through-silicon vias* (TSVs). TSVs are vertical wires that carry power and signals between different dies, which are etched in the silicon substrate between the 2D dies.

In this survey, we primarily target 3D stacked ICs with several digital logic dies and TSV-based interlayer communication. We refer to the targeted 3D ICs throughout this review by 3D multiprocessors systems-on-chip, or 3D MPSoCs.

3D MPSoCs are multi-layered stacked 3D ICs, where each die contains a number of processing units, memory modules, and other peripheral and interconnection units. Examples of typical 3D MPSoCs integrate a number of processing layers that contain all the processing units, and a number of memory layers. Another 3D MPSoC example is where the processing units and the memory modules are co-placed in each die of the 3D stacked layers. These examples have been shown in previous works [12, 13], and are shown in Fig. 1.2, which includes an UltraSPARC T1 [14] version of a 3D MPSoC. This vertical integration of logical modules brings several benefits to multi-core architectures, which are as follows:

- Vertical stacking shortens the wiring length between two modules. In this respect, the propagation delays, which are recently dominated by interconnect delays [15], are dramatically reduced leading to an increased performance of 3D MPSoCs. Thus, 3D MPSoCs would outperform 2D MPSoCs.

- 3D MPSoCs allow heterogenous integration of different components, such as DRAM on multi-core architectures [13]. 3D MPSoCs enhance the memory access bandwidth and throughput, by bringing the memory modules (e.g. DRAM) to the top or bottom

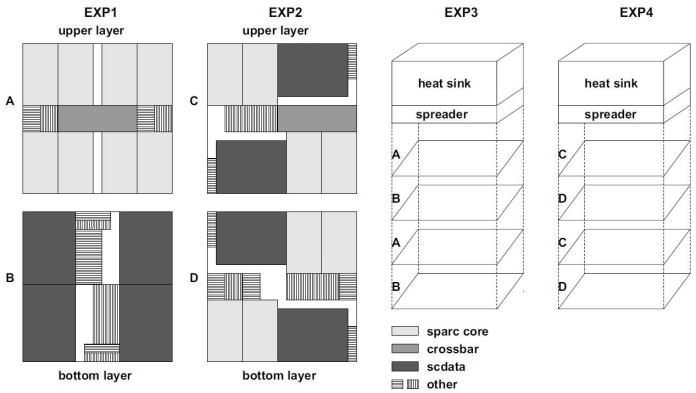


Figure 1.2: Schematic view of a 4-tier 3D MPSoC with different architectures [12].

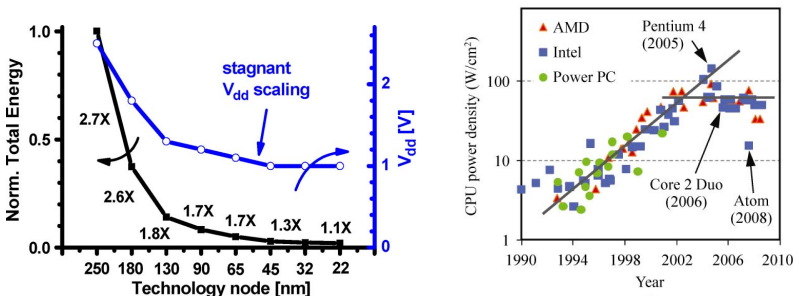
of processing layers. This would enable high-speed, massively-parallel data access to these stacked DRAM layers.

1.2 Thermal Issues in 3D MPSoCs

Despite the performance and throughput enhancements that 3D MPSoCs bring, 3D MPSoC designs face major challenges, particularly in the extreme elevated temperatures accompanied with high-performance designs.

While technology continues to scale-down the transistor features, MPSoCs voltage supply (V_{dd}) could not be scaled down accordingly [16]. Recent work [17] (Fig. 1.3(a)) has shown that the supply voltage scaling is saturating that, if combined with increased integration within a unit area due to reduced transistor features, leads to an increase in power consumption. In this respect, multi-core architectures design trends have taken the direction of increasing the power density by integrating more processing units on the chip (with a fixed chip area), as shown in Fig. 1.3(b). If the MPSoC power density keeps increasing, it will eventually reach the same magnitude of nuclear power plants [4, 18].

With such increased power densities, MPSoCs face a tremendous

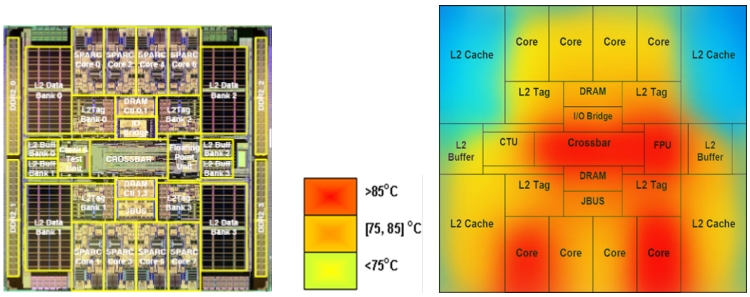


(a) Voltage and energy scaling (b) Power density scaling

Figure 1.3: Voltage/Energy [17] and power density [18] scaling trends.

increase in heat generation that has a direct impact on the lifetime of MPSoCs. This increased heat generation leads to high temperature in the MPSoCs. While high-frequency single processing units have faced the similar case of high temperatures, the thermal profile of MPSoCs can have a more severe impact. This is mainly related to the localized heat generation of the several processing units of MPSoCs. Thus, the localized heat generation creates several localized high temperatures, which is known as thermal *hot spots*. The existence of several thermal *hot spots* would imply that there are other localized cold spots, which leads to the creation of the undesirable spatial *thermal gradients*. Moreover, the time-varying nature of workload processing requirements, or even when the processing goes to power-up and power-down cycles, leads to temporal *thermal cycles* [19] formation. To demonstrate the MPSoC thermal issues, an example of various hot spots location and thermal gradient is shown in Fig. 1.4(b). This figure shows a thermal response snapshot of the UltraSPARC T1 (Niagara) [20] MPSoC to a typical workload execution.

While high-density 2D MPSoCs face strong thermal challenges, these challenges are more prominent in the vertically-stacked 3D MPSoCs [21, 12]. Due to the vertical stacking of different dies, the thermal resistance of 3D MPSoCs is significantly increased to alarming values [12], compared to the increased temperature we demonstrate in the case of 2D MPSoCs. This is mainly due to the increased and non-



(a) Layout (b) Temperature

Figure 1.4: Floorplan layout and thermal response of the UltraSPARC T1 MPSoC [20].

uniform thermal resistance at different stacked layers, based on their relative heat dissipation paths using conventional techniques such as placing heat sink on top of the top-most layer. For example, Fig. 1.5 shows the temperature of an emulated 3D MPSoC. This emulator is built by stacking 4 heat dissipation tiers on a substrate tier. In each of the heat dissipation tiers there is a number of controllable micro-heaters that are used to emulate the heat generation pattern of processing units similar to the actual pattern of each processing unit. In addition to these micro-heaters, there is a number of thermal sensors to capture the thermal profile of this emulator. This 3D thermal emulator has a heat sink placed at the top-most layer. The temperatures shown in this figure indeed confirm the expected high temperature and thermal gradient values of prospective high-performance 3D MPSoCs.

Thus, it is expected that high-density high-performance 3D MPSoCs are more prone to hot spots and thermal gradients. The existence of hot spots, thermal gradients, and thermal cycles heavily affect the MPSoC (2D and 3D) operation and lifetime, as shown in the following section.

1.3 Thermal Impact on 3D MPSoC Reliability and Performance

High temperature is undesirable in 3D MPSoCs operation due to the different device and interconnect reliability and degraded performance

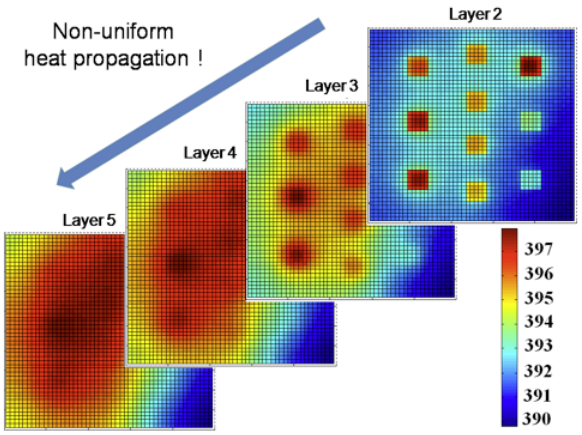


Figure 1.5: Thermal state of a 5 tier (4 thermal dissipating tiers + 1 substrate base tier) high-density MPSoC thermal emulator. Temperature values are in Kelvin [22].

sources that are highly affected, directly and indirectly, by this rise in temperature. These sources would affect the reliability of 3D MPSoCs by accelerating the processor aging or the *Mean-Time to Failure* (MTTF) [23], which is the statistical average time for the MPSoC to breakdown permanently, as well as creating irreversible functional failures in the computation modules (e.g., storage) that limit the full utilization of these modules. In addition to the impacted reliability, high 3D MPSoC temperature would eventually lead to degraded performance by reducing the operating frequency due to increased propagation delays or reduced energy-efficiency resulted from the increased leakage power consumption. Thus, it is important to identify the temperature-induced reliability and degraded performance sources and elaborate more on their corresponding impact. The following paragraphs give an overview of these sources:

Bias Temperature Instability (BTI) [24]. This factor causes instabilities in the device behavior, due to the stress applied on the bias (e.g., a negative bias on the gate source voltage of a PMOS transistor). BTI can be split to two types, namely Negative BTI, which is related to the PMOS device stress, and Positive BTI, which is related to the NMOS device stress. The main degraded parameter due to BTI is the

threshold voltage, as shown in prior work [24]. The change in threshold voltage during stress (increase in threshold voltage) and release times (decrease in threshold voltage) has a dependency on a number of factors, which includes temperature [25]. Higher operating temperatures indeed have a direct impact on the threshold voltage based on BTI, which results in longer circuit delays and increase in dynamic power consumption.

Hot-Carrier Injection [26]. Hot-carrier injection occurs when a carrier gains enough energy to tunnel from the transistor source or drain to the dielectric material. This even accompanied with a rise in the device temperature. Hot-carrier injection occurs at normal temperature range, but the injection rate is increased as the operating (or stress) temperature is increased [27]. Based on the above observations, hot-carrier injection could lead to thermal positive feedback loop situation, i.e., the injection leads to increase in temperature that may trigger an increase in the injection rate. Consequently, hot-carrier injection would lead to thermal run-away.

Time-Dependent Dielectric Breakdown (TDDB) [28, 29] in high-k device dielectric and low-k interconnect dielectric. This is modeled as trap generated that leads to a leakage path through the oxide layer of the transistor. This is also referred in literature as *gate oxide breakdown*. TDDB has an exponential dependency on temperature [28] that accelerates the failure of a transistor by breaking down the dielectric, hence forming a constant conducting path. As a consequence, the faulty transistor would be permanently in a conducting state.

ElectroMigration (EM) in metallic interconnect [30]. Electromigration is a phenomenon that occurs in the IC interconnects (metal layers) due to high current densities. EM leads to a shift in the conducting ions location, hence causing a breakdown in the interconnects. EM has a strong dependency on the temperature resulted from the utilization of the IC and the joule self-heating of the interconnects due to the high current density. In this respect, higher operating temperatures would

eventually lead to a breakdown of the metal layer, which may result in a complete failure of the IC.

Subthreshold Leakage Current [31]. Subthreshold leakage current is one of the sources of leakage current, and hence static power consumption in MPSoCs. It is the drain-source current of a transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is due to the diffusion current of the minority carriers in the channel. Subthreshold leakage is found to be the dominant component in the overall leakage current sources [32]. Subthreshold leakage current has a strong dependency on the operating temperatures with a sensitivity of $8 - 12x/100^oC$ [31].

The aforementioned sources can lead to system failure if no proper measures are taken. But these sources also degrade the MPSoCs (2D and 3D) operation from its original (also called time-zero) operating conditions. The following paragraphs highlight more on these affected parameters:

Mean-Time To Failure [23, 31]. The mean-time to failure would be heavily impacted due to the temperature impact on Time-Dependent Dielectric Breakdown (TDDB), Electromigration (EM), as well as stress migration and thermal cycling.

Temperature-Dependent Propagation Delays [33]. This change in the time required for a signal to travel between two modules is related to the thermally-induced delays in the logic gates (e.g. resulted from BTI), as well as the increase of the interconnect resistivity (e.g. resulted from Electro-migration). Another cause for the propagation delay is in the clock skew between different modules experiencing diverse thermal stress. In this respect, propagation delays have a strong dependency not just on the overall thermal state of the IC, but on the spatial thermal gradient as well. Indeed, previous work reports that a spatial gradient of 40^oC would create a 10% clock skew between different modules within a single IC.

Temperature-Dependent Leakage Power [31]. Leakage power is one of the sources of static power consumption in MPSoCs. The leakage power is a cause of various elements, such as the reverse-biased junction leakage current and the subthreshold leakage. These elements have a strong dependency on the operating temperatures. In fact, it has been shown by previous work that the leakage power has an exponential [34] dependency on temperature. Thus, it is crucial to prevent the operating MPSoCs from entering thermal runaway situations. Temperature-dependent leakage power may not be viewed as a failure mechanism, but high leakage power would cause a significant degradation in the power efficiency, as it would surpass the dynamic power consumption, where dynamic power is the effective power used in computations and is mainly workload dependent.

1.4 Advanced Cooling Technologies for 3D MPSoCs

To address the increasing thermal rise of 3D MPSoCs, several research initiatives have explored several advancing cooling strategies for the target architectures. For instance, there has been several research efforts to insert dummy thermal through-silicon vias (TTSVs) [35] to dissipate the heat generated from the layers further from the heat sink in a more efficient way.

Another advanced cooling technology uses injected fluids (single- or two-phase), between the different layers of the 3D MPSoCs. This cooling methodology, which is also known as interlayer liquid cooling [36], is achieved by manufacturing a cavity layer, for example rectangular microchannels or micro pin-fin structures [37], on the back-side of each silicon layer. A typical structure of 3D MPSoCs consists of two or more silicon tiers, which contain the processing and storage elements of the system. The communication between these tiers is realized with through-silicon vias (TSVs) that are etched in the residual silicon slab. To account for inter-tier liquid cooling, the porous cavity is realized by etching porous structures of different form and shapes (cf. Fig. 1.6). In the example shown in Fig. 1.6, the micro-channels are built, and distributed uniformly, in between the vertical layers for liquid flow. The

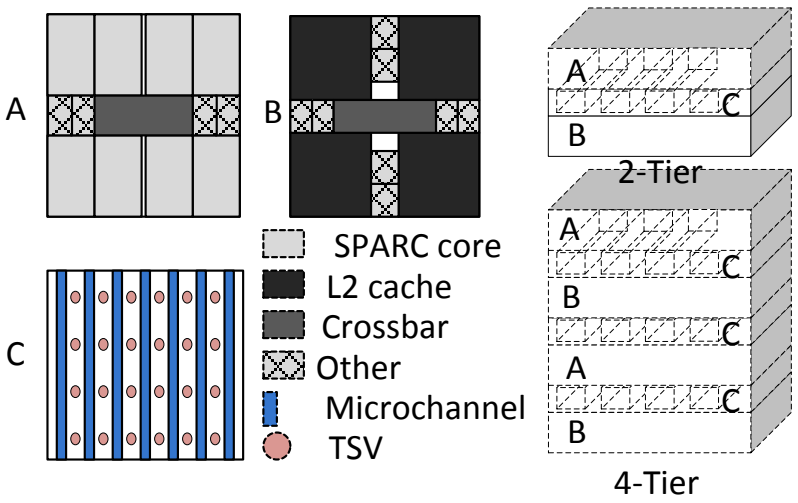


Figure 1.6: Layouts of the interlayer liquid-cooled 3D MPSoCs [38].

fluid flows through each channel at the same flow rate, but the liquid flow rate provided by the pump can be dynamically altered at runtime.

Manufacturing 3D MPSoCs with TSV interconnections and microchannels requires a series of microfabrication processes, namely (1) deep-reactive-ion-etching (DRIE) process for anisotropic silicon etching of both TSV openings and backside microchannels (cf. Fig. 1.7); (2) conformal thin film deposition for TSV sidewall insulation; (3) electroplating for conductive layer formation; (4) grinding for chip thinning, and finally (5) wafer- or die-level bonding for the stacking. A simplified illustration of a 3D stack with inter-tier liquid cooling is shown in Fig. 1.8.

Despite the benefits that liquid cooling brings in terms of significant thermal reduction, liquid cooling adds additional challenges to obtain a balanced thermal state with low spatial thermal gradients. As the coolant flows in microchannels, it experiences sensible heat absorption along the path [41]. This results in the coolant temperature increase from inlet to outlet, which causes a thermal gradient formation on the MPSoC surface even when the heat dissipation is uniform, as shown in Fig. 1.9(a). More commonly, in 3D MPSoCs with non uniform heat

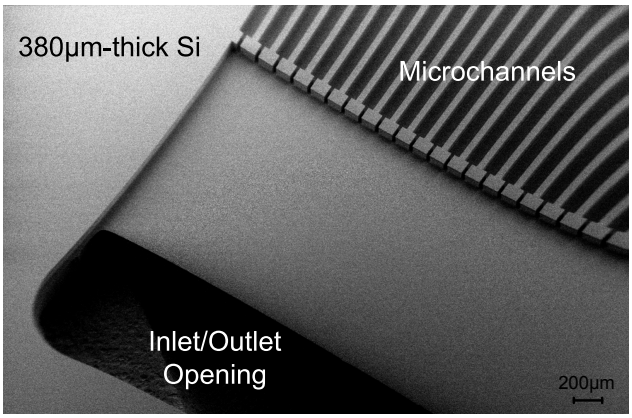


Figure 1.7: SEM photos the wafer Back-side with the inlet-outlet openings while showing the micro-channels [39].

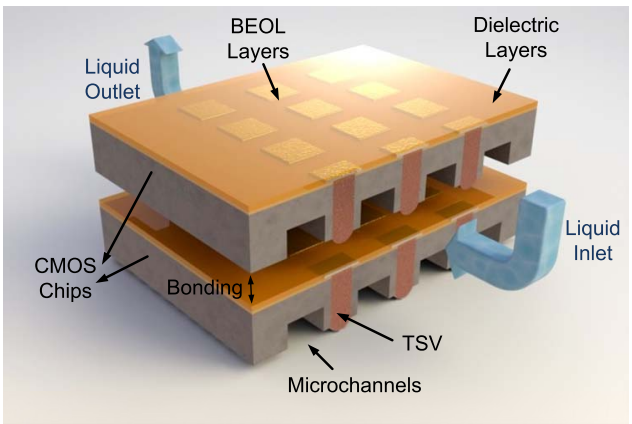
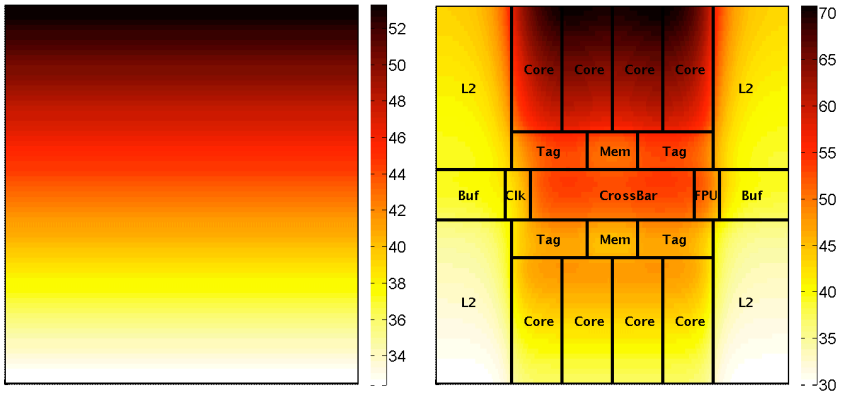


Figure 1.8: Simplified illustration of 3D stack with inter-tier liquid cooling [39].

dissipations, the existing thermal gradients and hot spots are aggravated by this characteristic of interlayer liquid cooling, as shown in Fig. 1.9(b). As a result, thermal gradients proliferate in 3D MPSoCs with liquid cooling. These gradients cause uneven thermally-induced stresses on different parts of the MPSoC, significantly undermining overall system reliability [31] (cf. Section 1.3.

From these observations we deduce that these new advanced cooling technologies bring both additional benefits and challenges. Thus,



(a) Uniform heat flux (b) UltraSPARC T1

Figure 1.9: Steady-state temperature distribution of a 14mm x 15mm two-die 3D IC with (a) uniform (combined) heat flux density of 50W/cm^2 and (b) the UltraSPARC T1 (Niagara-1) chip architecture [14]- the (combined) heat flux densities range from 8W/cm^2 to about 64W/cm^2. Direction of the coolant flow is from the bottom to the top of the figure [40].

it is crucial to find an optimized methodology to apply these technologies, alongside conventional 2D temperature balancing techniques in the context of resource-efficient temperature-aware 3D MPSoCs. Our interest in resource-efficiency varies from area to applied energy.

1.5 Survey Overview and Outline

In this survey, we provide an extensive survey that covers temperature-aware design optimizations and run-time management schemes for 3D MPSoCs, to avoid the rapid degradation of these architectures due to the thermal impact on reliability. The survey shows how the state-of-the-art tackles the thermal issues in the emerging 3D MPSoCs that include advanced cooling mechanisms, such as thermal-through-silicon-vias (TTSVs) and interlayer liquid cooling. We perform this survey exploration in a top-down manner to cover all the temperature-aware aspects in the target architecture. In particular, we provide two main research directions that tackle the thermal issues, namely:

1. **Design-time technological solutions and temperature-aware optimizations**. In this category we explore various techniques that address, at *design-time*, the means of generating and dissipating heat in 3D MPSoCs. This includes the optimization of new advanced cooling and heat dissipation mechanisms, temperature-aware floorplanning, and design-time optimization of different parameters that would affect the thermal behavior of 3D MPSoCs.

2. **Run-time thermal management mechanisms**. We show in this category the various temperature-affecting knobs in the target 3D MPSoC, and how the state-of-the-art utilizes these knobs in developing several *run-time* thermal management mechanisms.

1.5.1 Related Survey Works

Our proposed survey overlaps with several surveys that exist in literature. An initial survey in thermally-aware design [42] explores the various design-optimization mechanisms for MPSoCs, both planar 2D and vertical 3D. In particular, this previous survey explains the various modeling framework approaches and explores thermal-aware floorplanning, and the means to recover from temperature-induced parameters degradation such as run-time shifts. However, there is no exploration for advanced cooling mechanisms, other design-time optimization mechanisms, or run-time thermal management techniques, which are explored in our proposed survey.

There is a recent survey work that explores various thermal management mechanisms for processing architectures [43]. In this previous survey, several mechanisms for balancing temperatures in 2D and 3D MPSoCs are explored, namely thermal sensor placement, run-time thermal management, floorplanning, operating system/compilation techniques, and a brief exploration on liquid cooling. However, this survey does not provide a systematic classification of the temperature optimization research field. In our proposed survey, however, we provide our classification in a more systematic methodology that follows a top-down reasoning to cover most of the research directions in 3D MPSoC

temperature optimization.

Finally, another survey explores thoroughly vertical integration in 3D ICs [44]. This previous work explores the various electronic-design automation tools needed for 3D architectures. Then it explores the various architecture flavors in 3D ICs, namely 3D field programmable gate arrays (FPGA) and 3D MPSoC designs. Thus, this previous survey work is complementary to our proposal.

1.5.2 Survey Organization

This survey starts with providing an overview of the recent thermal modeling approaches developed for the target 3D MPSoC architectures in Section 2. In Section 3, we explore the design-time optimization schemes to minimize the temperature-oriented issues in 3D MPSoCs. Section 4 shows our exploration in run-time thermal management schemes for 3D MPSoCs. We first start by stating the various temperature-affecting control knobs, then we show the classification of different management schemes that use these knobs to balance the dissipated heat in the target architecture. Finally, we summarize our work in this survey in the conclusion.

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