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Discrete Circuit Optimization: Library Based Gate Sizing and Threshold Voltage Assignment

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Discrete Circuit Optimization: Library Based Gate Sizing and Threshold Voltage Assignment

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Abstract

Discrete gate sizing and threshold assignment are commonly used tools for optimizing digital circuits, and ideal methods for incremental optimization. The gate widths and threshold voltages, along with the gate lengths, can be adjusted to optimize power and delay. This monograph surveys this field, providing the background needed to perform research in the field. Concepts such as standard cell libraries, static timing analysis, and analytical delay and power models are explained, along with examples and data to help understand the tradeoffs involved. Comparative results are also provided to show the current state of the field.

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1

Introduction

Gate sizing and threshold voltage assignment[1] are widely used to optimize digital circuits. They can be used to manage trade-offs in power, timing, area, yield, crosstalk, statistical power, statistical delay and soft-errors. They can also be used incrementally and as a method for optimizing post-layout designs after placement and interconnect routing. After over three decades, research is still active in the area.

This work will consider the case of gate sizing and threshold voltage assignment for standard library cell designs. In this context, gates are chosen from a library of pre-characterized gates that act as the fundamental building blocks. Cell-based designs compose the majority of the digital designs today.

1.1 Other Types of Cell Optimization Problems

There are other variants of gate sizing and threshold voltage assignment that are not covered in this work:

(1) Transistor sizing for analog design
(2) Transistor sizing for custom digital design

[1] While the title explicitly states the gate sizing and V_t assignment, the material is relevant to other cell optimization methods, such as gate-length biasing problems.

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These variants are a minority of IC designs. Custom digital design is mainly limited to high-performance designs. However, analog designs are becoming increasingly important with the increase in systems on a chip (SoC) methodologies that integrate entire TVs or radios on a single die [63].

1.1.1 Transistor Sizing for Analog Designs

In analog design, there are many different constraints and performance specifications: gain, accuracy, linearity, signal-to-noise, and impedance matching. For example, the pair of transistors forming a current mirror or differential pair must be *matched*, or have very similar electrical characteristics. Also, transistors that function as voltage-controlled resistors must be operating in the linear region, and an amplifier must have the proper signal-to-noise ratio for the system to work properly. While standard cells mask much of the underlying electrical waveforms using logic states, analog designs utilize these underlying characteristics to produce amplifiers, digital-to-analog converters, current sources, etc. However, many more facets of the design must be controlled for a proper function.

The main challenge in automated analog sizing is to input the design specifications and models into a form that can be used by the sizing method. This is challenging because the range of analog designs is large. For instance, while the analytical performance models for a given op-amp topology might be well known, it is difficult to write down the equations that govern the sizing of an *arbitrary* design.

Early methods for automated sizing were *knowledge-based*, where templates [52, 55, 72] were used to synthesize designs. These pre-characterized templates would carry information on a good initial sizing and on how to optimize the given template. Sizing these designs was therefore equivalent to executing the design plans. For example, in [52], the sizing proceeds by determining the bias current, then the W/L ratios, followed by the $1/f$ noise consideration, and finally the W and L of each device. In [72], the values are chosen using a fixed point method, where the parameters are determined serially. Each parameter is chosen to best satisfy the design considerations, assuming the other parameters to be fixed.

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The time required to construct these templates, however, was often much greater than the time needed to design the circuit directly [63]. The accumulation of knowledge bases, and the codification of the expert knowledge was not practical. This, coupled with the limited range of circuits that the method could handle, led to the decline of these types of methods. However, there is recent interest in automating the knowledge-extraction process [108], and in identifying substructures in a design automatically [107].

Another branch of analog sizing is the *optimization-based* methods. These methods use optimization procedures, rather than codified design rules, to size the design. The first subclass of optimization methods consists of *equation based methods*[2] [64, 75, 87] that rely on the designer to provide the equations, but in contrast to the knowledge-based methods, the sizing process is automated using optimization methods, rather than rules. The optimization process may use simulated annealing [64], steepest-descent [87], or convex optimization [75]. This sub-class works well in certain contexts (such as in [75]), but they may be limited by their accuracy.

The second subclass of optimization based methods are the *simulation based methods* [54, 58, 88, 118, 119, 126] that use numerical simulations to measure the performance. The simulations provide these methods with greater accuracy, however they create a large overhead that makes these methods much slower than their equation-based counterparts.

1.1.2 Transistor Sizing for Custom Digital Designs

In the custom digital setting, every transistor in the design is available for optimization [7, 44, 45, 82, 153]. The early papers on gate sizing were based on transistor-level sizing (see [60, 135]), until standard cells became widespread in the 1990s.[3] With the increasing complexity of designs, standard cell libraries are almost universally used.

Custom digital design techniques are primarily used for high-performance parts of high-volume designs which is needed to recover

[2] See [63] for the taxonomy of analog sizing methods and a comprehensive review of methods prior to 2000.
[3] See, for example, [159].

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the increased cost of designing at a transistor level, as in the case of microprocessors [12]. Custom digital transistor sizing is still an active area of research today and most current research is directed toward the statistical design of custom circuits [8, 43, 146]. However, these methods account for a minority of the digital designs.

1.2 The Physical Design Process

Gate sizing and threshold voltage assignment are a part of the larger Electronic Design Automation (EDA) ecosystem that transforms Register Transfer Language (RTL) descriptions into a physical layout. The process of creating the physical layout is called the *physical design* process, and consists of six steps:

(1) **Logic synthesis**.
   - Input: RTL/HDL design description, standard cell library information, timing constraint information.
   - Output: Netlist mapped to the standard cell library.

   Transform the RTL/HDL design description into a gate level netlist, using a given cell library. Convert state machines, map arithmetic blocks, etc.

(2) **Floorplanning**.
   - Input: synthesized netlist, macro information, standard cell library information, standard cell row information, information on chip inputs and outputs.
   - Output: floorplan with rows for standard cell placement, pads for input and output, locations for macros.

   Create a die for the design, and allocate space for input–output ports, macros, and library gates.

(3) **Placement**.
   - Input: synthesized netlist, floorplan.
   - Output: locations for each of the cells in the design in a standard cell row.

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Places, flips and rotates cells into the rows created by the floorplanning algorithm. Minimizes the wirelength in the resulting layout, while meeting timing constraints (timing-driven placement).

(4) **Clock Tree synthesis**.

- Input: placed design, clock nets.
- Output: clock tree to distribute the clock signal to the sequential elements (flip-flops, latches, etc.).

Creates a clock tree to distribute the clock signal across the design. The goals are to minimize the size of the clock tree (to minimize power), and the skew at each of the outputs of the clock tree. Buffers may be added to help distribute the clock signal.

(5) **Routing**.

- Input: placed design, connection information, metal and via information from the library.
- Output: design with cells connected with wires.

Connects cells in the library using metal layers and vias. The objective is to minimize the amount of interconnect needed, while observing design rules and meeting timing.

(6) **Physical verification and yield enhancement**.

- Input: placed, routed design.
- Output: verified design with improved yield.

Improves the yield of the design. Corrects design rules violations, inserts metal fill, doubles vias, checks connectivity and topology.

A flowchart for the EDA process is shown in Figure 1.1.

Although gate sizing and threshold voltage assignment are not explicitly in the design flow above, they are used throughout the design flow to correct timing errors, and to optimize the design. For example, they are commonly used after placement to resize gates that violate maximum fanout rules or flip-flop setup time requirements (see, for example [22]). After clock tree synthesis, they are used to further fix

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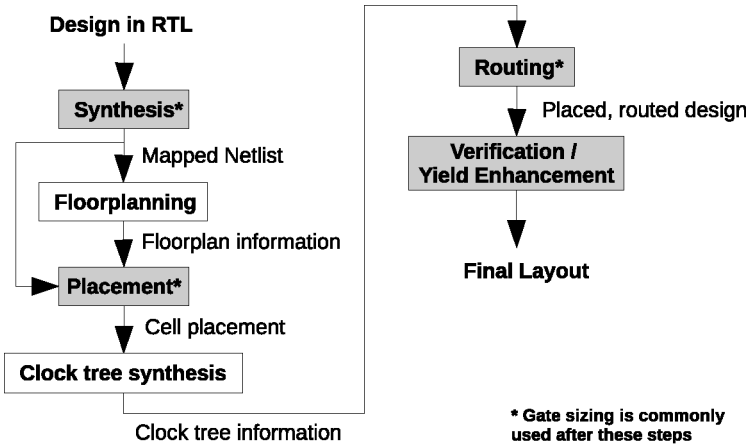

Fig. 1.1 Electronic Design Automation flow.

rule violations and setup and hold violations, using the clock information from the clock-tree synthesis. After routing, they are again used to fix setup and hold violations, along with design rule violations. At this step, an incremental routing may be needed to account for changes in the cell sizes, and their corresponding pin locations.

They are also used at different points in the design flow to reduce the power consumption [2]. While this may reduce the power *using the same timing constraint*, in other instances the timing constraints may need to be relaxed to achieve a power reduction.

Gate sizing and threshold voltage assignment are powerful tools for optimization, and are the most widely used incremental optimization tools. These methods are more powerful and less intrusive than adjusting the placement or routing of the design. For example, fixing setup time violations using placement would require the gates on the violating path to be moved, and would require rerouting the interconnects. Similarly, fixing setup time violations using routing would also require the connections between the cells to be rerouted. In both the cases, a significant portion of the design will need to be rerouted to provide benefits.

On the other hand, gate sizing and threshold voltage assignment are less disruptive than re-placing the cells or re-routing them. For example, the timing of a buffer driving a large wire load could be improved

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by increasing its size. This may result in a local rerouting to accommodate the different pin locations of the larger cell, and if there is no space around the surrounding cell, then an incremental placement will be needed to create space for the cell. However, this is preferable to rerouting large sections of the design, or adjusting the placements of tens or hundreds of cells.

In some cases, when only the gate lengths or threshold voltages change, the disruption is very minimal. In these cases, the cell dimensions and pin locations are the same, and these cell alternatives can be swapped without any change in the routing or the placement. The only verification needed is to ensure that the crosstalk noise, power, and timing constraints are satisfied.

Another advantage of gate sizing and threshold voltage assignment is that they are *versatile*, as they can be targeted to different optimization objectives. They have been used for power and timing optimization [46], to fix noise constraints due to crosstalk [98, 170], to harden soft-errors due to radiation [174], to improve yield [37, 50], and to minimize statistical power [42, 151].

1.3 The Standard Cell Library

The standard cell library contains logic cells such as inverters, ands, not–ands (nands), and x-ors that implement Boolean logic functions. There are also sets of sequential cells such as flip-flops, latches, and their variants with capabilities for setting, resetting and reading in scan-chains. These sequential cells provide *memory*, allowing pipe-lining, state machines, and a memory for computations. Lastly, there are utility cells, such as filler cells, antenna cells, and buffer cells, which are tools to help with the physical implementation of the design.

The library generally provides several gate options for each logic function. Each of the options are logically equivalent — they implement the same boolean function — but have varying electrical characteristics, due to differences in their gate lengths, widths, PMOS–NMOS width ratios and threshold voltages V_t. These alternative options can be used to optimize the design. For example, critical paths can be sped up by swapping high-V_t cells by low-V_t cells, and gates with fanout violations

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can be fixed using alternatives with larger-transistor widths and smaller effective resistances at the gate outputs.

Two library files that are used for sizing and threshold voltage assignment are:

(1) **Physical library information.**
(usually expressed in Library Exchange Format (LEF)):
- Cell information: dimensions of the cell and locations of the pins.
- Interconnect information: dimensions, pitch, capacitance, and resistances for each metal layer.
- Via information: dimensions, resistance, and layers that are connected.

(2) **Timing library information.**
(usually expressed in Liberty Format):
- Library characterization information: temperature, voltage and process.
- Parameters used in the library: slew thresholds, input thresholds, output thresholds, and measurement units.
- Cell information: delays, area, logic function, short-circuit power, switching power, leakage power. For flip-flops the hold and setup time requirements are also given.
- Cell pin information: capacitances, maximum loads.

The geometry information in the LEF file is used for placement and routing. This information tells the program how to create standard cell rows for floorplanning, and the dimensions of each cell for placement. Next, the pin locations, interconnect geometries, and via dimensions are used for routing, and once routing is complete, the capacitance and resistance information is used to extract information about the wire parasitics.

The timing and power information from the Liberty file is used for the timing and power analysis of the design. The timing information

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is used in conjunction with the wire parasitic information to create delay estimates and power estimates with interconnect loading modeling. This will be covered in more detail in Section 2.4.

1.4 The Gate Sizing and V_t Assignment Problem

Of the many variations on the gate sizing and threshold voltage assignment problem, this work will consider the following metrics:

- Leakage power
- Dynamic power
- Clock period

The application most commonly found in literature today is to minimize the power, or some combination of the leakage power and the dynamic power, with a constraint on the clock period. When timing closure is important, the objective is to minimize the clock period, and in post-layout situations, the noise and crosstalk violations are often optimized.

The variables in the optimization process are the cells used to implement the gates. These cells can be swapped to decrease the delay or power, or to modify the output signal waveform. The cells may be different sizes, and have different pin locations.

Functionally equivalent cells that can be interchanged may be identified by the designer, the design tool, or by the library by having the same *footprint*. For example, the inverter-type cells will have an "inverter" footprint, which identifies the family of cells that can be used to replace the gate. Each of these cells performs the same logic function, thus changing the cells does not affect the functionality of the design.

Formally, the problem may be written as an optimization problem. For example, with the vector of cell options $\vec{\omega}$, the delay-constrained power optimization problem is:

$$\begin{aligned} &\text{minimize} && \text{Power}(\vec{\omega}) \\ &\text{subject to} && \text{Delay}(\vec{\omega}) \leq T_{\max} \end{aligned} \tag{1.1}$$

where $T_{\max}$ is the clock period. This form helps summarize the objectives and constraints in the optimization process.

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Table 1.1. Notation.

Symbol	Meaning
$\mathcal{G}$	Set of gates in the design
g	A gate in the design
ω, ω_0	A cell option, current cell option
CellOptions(g)	Set of alternative library cell options for g
w_g	The width for gate g
$v_{\text{th}\,g}$	The threshold voltage for gate g
t_a	Arrival time
$t_{a(g)}$	Set of arrival times for the inputs of gate g
t_r	Required arrival time
$t_{r(g)}$	Set of required arrival times for the inputs of gate g
τ_g	Set of input transition slews for gate g
d	Delay
p	Power
PI	*Primary inputs* input ports in the design
PO	*Output ports* in the design
fi(g)	The set of gates that drive the inputs of gate g
fo(g)	The set of gates that are connected to the output of gate g
ϵ	A small positive number
ρ	Power/delay tradeoff sensitivity

The delay is estimated using a Static Timing Analysis method (see Section 2) and timing constraints are usually expressed in a Synopsys Design Constraint (SDC) format. These constraints can be very complex, with multicycle paths, multiple clocks, power domains, and false-path definitions. In addition, parasitic information in a Standard Parasitic Exchange (SPEF) format is used to approximate the interconnect delay.

1.5 Notations and Acronyms

While new notation is avoided when possible, notation for certain key concepts are unavoidable. The notation for key symbols used in this monograph are summarized in Table 1.1. These symbols, and concepts, will be elaborated in the remainder of the monograph; for example, the slew and other timing concepts will be covered in the following section.

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References

[1] A. Abou-Seido, B. Nowak, and C. Chu, "Fitted Elmore delay: a simple and accurate interconnect delay model," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 12, no. 7, pp. 691–696, 2004.

[2] H. Abrishami, J. Lou, J. Q. J. Froessl, and M. Pedram, "Post sign-off leakage power optimization," in *Proceedings of Design Automation Conference*, 2011.

[3] A. Agarwal, D. Blaauw, V. Zolotov, S. Sundareswaran, M. Zhao, K. Gala, and R. Panda, "Statistical delay computation considering spatial correlations," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 271–276, 2003.

[4] A. Agarwal, K. Chopra, and D. Blaauw, "Statistical timing based optimization using gate sizing," in *Proceedings of Design, Automation and Test in Europe*, pp. 400–405, 2005.

[5] C. Amin, N. Menezes, K. Killpack, F. Dartu, U. Choudhury, N. Hakim, and Y. Ismail, "Statistical static timing analysis: How simple can we get?," in *Proceedings of Design Automation Conference*, pp. 652–657, 2005.

[6] Available on http://www.opencores.org.

[7] X. Bai, C. Visweswariah, P. Strenski, and D. Hathaway, "Uncertainty-aware circuit optimization," in *Proceedings of Design Automation Conference*, pp. 58–63, 2002.

[8] D. K. Beece, J. Xiong, C. Visweswariah, V. Zolotov, and Y. Liu, "Transistor sizing of custom high-performance digital circuits with parametric yield considerations," in *Proceedings of Design Automation Conference*, pp. 781–786, 2010.

Full text available at: http://dx.doi.org/10.1561/1000000019

[9] F. Beeftink, P. Kudva, D. Kung, and L. Stok, "Gate-size selection for standard cell libraries," in *Proceedings of the International Conference on Computer-Aided Design*, pp. 545–550, November 1998.
[10] R. Bellman, *Dynamic Programming*. 1957.
[11] M. R. C. M. Berkelaar and J. A. G. Jess, "Gate sizing in mos digital circuits with linear programming," in *EURO-DAC '90: Proceedings of the Conference on European Design Automation*, pp. 217–221, 1990.
[12] R. Berridge, R. Averill, A. Barish, M. Bowen, P. Camporese, J. DiLullo, P. Dudley, J. Keinert, D. Lewis, and R. Morel et al., "IBM POWER6 microprocessor physical design and design methodology," *IBM Journal of Research and Development*, vol. 51, no. 6, pp. 685–714, 2007.
[13] D. Bertsekas, *Dynamic Programming and Optimal Control*, vol. I. Athena Scientific, 2005.
[14] J. Bhasker and R. Chadha, *Static Timing Analysis for Nanometer Designs: A Practical Approach*. Springer Verlag, 2009.
[15] D. Blaauw, K. Chopra, A. Srivastava, and L. Scheffer, "Statistical timing analysis: From basic principles to state of the art," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 4, pp. 589–607, 2008.
[16] K. Boese, A. Kahng, B. Mccoy, and G. Robins, "Fidelity and near-optimality of Elmore-based routing constructions," in *Proceedings of International Conference on Computer Design*, pp. 81–84, 1993.
[17] S. Boyd, S. Kim, D. Patil, and M. Horowitz, "Digital circuit optimization via geometric programming," *Operations Research*, vol. 53, no. 6, p. 899, 2005.
[18] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge University Press, 2004.
[19] R. Brawhear, N. Menezes, C. Oh, L. Pillage, and M. Mercer, "Predicting circuit performance using circuit-level statistical timing analysis," in *Proceedings of the European Conference on Design Automation (EDAC). European Test Conference (ETC). The European Event in ASIC Design (EUROASIC)*, pp. 332–337, 1994.
[20] F. Brglez, D. Bryan, and K. Kozminski, "Combinatorial profiles of sequential benchmark circuits," in *Proceedings of International Symposium on Circuits and Systems*, pp. 1929–1934, May 1989.
[21] S. M. Burns, M. Ketkar, N. Menezes, K. A. Bowman, J. W. Tschanz, and V. De, "Comparative analysis of conventional and statistical design techniques," in *Proceedings of Design Automation Conference*, pp. 238–243, 2007.
[22] Cadence, "Encounter v. 10.11," Avalilable on http://www.cadence.com.
[23] M. Celik, L. Pileggi, and A. Odabasioglu, *IC Interconnect Analysis*. Springer Netherlands, 2002.
[24] P. Chan, "Algorithms for library-specific sizing of combinational logic," in *Proceedings of Design Automation Conference*, pp. 353–356, 1990.
[25] H. Chang and S. S. Sapatnekar, "Statistical timing analysis considering spatial correlations using a single pert-like traversal," in *Proceedings of International Conference on Computer-Aided Design*, p. 621, 2003.
[26] H. Chang, V. Zolotov, S. Narayan, and C. Visweswariah, "Parameterized block-based statistical timing analysis with non-Gaussian parameters,

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nonlinear delay functions," in *Proceedings of Design Automation Conference*, pp. 71–76, 2005.

[27] C. Chen, C. Chu, and D. Wong, "Fast and exact simultaneous gate and wire sizing by lagrangian relaxation," *IEEE Transactions on Computer-Aided Design*, vol. 18, no. 7, pp. 1014–1025, 1999.

[28] C. Chen and M. Sarrafzadeh, "Power reduction by simultaneous voltage scaling and gate sizing," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 333–338, 2000.

[29] C. Chen and M. Sarrafzadeh, "Simultaneous voltage scaling and gate sizing for low-power design," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 6, pp. 400–408, 2002.

[30] D.-S. Chen and M. Sarrafzadeh, "An exact algorithm for low power library-specific gate re-sizing," in *Proceedings of Design Automation Conference*, pp. 783–788, 1996.

[31] H. Chen and S. Kang, "iCOACH: A circuit optimization aid for CMOS high-performance circuits," *Integration, the VLSI journal*, vol. 10, no. 2, pp. 185–212, 1991.

[32] L. Cheng, J. Xiong, and L. He, "Non-linear statistical static timing analysis for non-Gaussian variation sources," in *Proceedings of Design Automation Conference*, pp. 250–255, 2007.

[33] D. Chinnery and K. Keutzer, *Closing the Power Gap between ASIC & Custom: Tools and Techniques for Low Power Design*. New York Inc.: Springer-Verlag, 2007.

[34] D. G. Chinnery and K. Keutzer, "Linear programming for sizing, vth and vdd assignment," in *Proceedings of International Conference on Low Power Electronics and Design*, pp. 149–154, 2005.

[35] B. Choi and D. Walker, "Timing analysis of combinational circuits including capacitive coupling and statistical process variation," in *Proceedings of VLSI Test Symposium*, pp. 49–54, 2000.

[36] S. H. Choi, B. C. Paul, and K. Roy, "Novel sizing algorithm for yield improvement under process variation in nanometer technology," pp. 454–459, 2004.

[37] K. Chopra, S. Shah, A. Srivastava, D. Blaauw, and D. Sylvester, "Parametric yield maximization using gate sizing based on efficient statistical power and delay gradient computation," in *Proceedings of International Conference on Computer-Aided Design*, pp. 1023–1028, 2005.

[38] K. Chopra, B. Zhai, D. Blaauw, and D. Sylvester, "A new statistical max operation for propagating skewness in statistical timing analysis," in *Proceedings of International Conference on Computer-Aided Design*, pp. 237–243, 2006.

[39] H. Chou, Y. Wang, and C. Chen, "Fast and effective gate-sizing with multiple-vt assignment using generalized lagrangian relaxation," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 381–386, 2005.

[40] W. Chuang, S. Sapatnekar, and I. Hajj, "Timing and area optimization for standard-cell VLSI circuit design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, p. 308, 1995.

[41] C. Clark, "The greatest of a finite set of random variables," *Operations Research*, vol. 9, no. 2, pp. 145–162, 1961.

Full text available at: http://dx.doi.org/10.1561/1000000019

[42] J. Cong, P. Gupta, and J. Lee, "Evaluating statistical power optimization," *IEEE Transactions on Computer-Aided Design*, vol. 29, no. 11, pp. 1750–1762, 2010.

[43] J. Cong, J. Lee, and L. Vandenberghe, "Robust gate sizing via mean excess delay minimization," in *Proceedings of International Conference on Physical Design*, pp. 10–14, 2008.

[44] A. Conn, P. Coulman, R. Haring, G. M. C. Visweswariah, and C. Wu, "JiffyTune: Circuit optimization using time-domain sensitivities," *IEEE Transactions on Computer-Aided Design*, vol. 17, no. 12, pp. 1292–1309, 1998.

[45] A. Conn, R. Haring, C. Visweswariah, P. Coulman, and G. Morrill, "Optimization of custom MOS circuits by transistor sizing," in *International Conference on Computer-Aided Design*, p. 174, 1996.

[46] O. Coudert, "Gate sizing: A general purpose optimization approach," in *Proceedings of Design, Automation and Test in Europe*, p. 214, 1996.

[47] O. Coudert, "Gate sizing for constrained delay/power/area optimization," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 5, pp. 465–472, December 1997.

[48] O. Coudert, R. Haddad, and S. Manne, "New algorithms for gate sizing: A comparative study," in *Proceedings of Design Automation Conference*, pp. 734–739, 1996.

[49] Z. Dai and K. Asada, "MOSIZ: A two-step transistor sizing algorithm based on optimal timing assignment method for multi-stage complex gates," in *Proceedings of Custom Integrated Circuits Conference*, pp. 17–3, 1989.

[50] A. Davoodi and A. Srivastava, "Variability driven gate sizing for binning yield optimization," in *Proceedings of Design Automation Conference*, pp. 959–964, 2006.

[51] A. Davoodi and A. Srivastava, "Variability driven gate sizing for binning yield optimization," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 16, no. 6, pp. 683–692, 2008.

[52] M. Degrauwe, O. Nys, E. Dijkstra, J. Rijmenants, S. Bitz, B. Goffart, E. Vittoz, S. Cserveny, C. Meixenberger, and G. Van der Stappen et al., "IDAC: An interactive design tool for analog CMOS circuits," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 1106–1116, 1987.

[53] A. Dharchoudhury, D. Blaauw, J. Norton, S. Pullela, and J. Dunning, "Transistor-level sizing and timing verification of domino circuits in the power pctm microprocessor," in *Proceedings of International Conference on Computer Design*, pp. 143–148, October 1997.

[54] A. Dharchoudhury and S. Kang, "Worst-case analysis and optimization of VLSI circuit performances," *IEEE Transactions on Computer-Aided Design*, vol. 14, no. 4, pp. 481–492, 1995.

[55] F. El-Turky and E. Perry, "Blades: An artificial intelligence approach to analog circuit design," *IEEE Transactions on Computer-Aided Design*, vol. 8, pp. 680–692, June 1989.

[56] W. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *Journal of Applied Physics*, vol. 19, pp. 55–63, 1948.

Full text available at: http://dx.doi.org/10.1561/1000000019

[57] P. Feldmann and S. Abbaspour, "Towards a more physical approach to gate modeling for timing, noise, and power," in *Proceedings of Design Automation Conference*, pp. 453–455, 2008.

[58] P. Feldmann and S. Director, "Integrated circuit quality optimization using surface integrals," *IEEE Transactions on Computer-Aided Design*, vol. 12, pp. 1868–1879, December 1993.

[59] P. Feldmann and R. Freund, "Efficient linear circuit analysis by pade approximation via the lanczos process," *IEEE Transactions on Computer-Aided Design*, vol. 14, pp. 639–649, May 1995.

[60] J. Fishburn and A. Dunlop, "TILOS: A posynomial approach to transistor sizing," in *Proceedings of International Conference on Computer-Aided Design*, 1985.

[61] C. Forzan and D. Pandini, "Statistical static timing analysis: A survey," *Integration, the VLSI Journal*, vol. 42, no. 3, pp. 409–435, 2009.

[62] A. Gattiker, S. Nassif, R. Dinakar, and C. Long, "Timing yield estimation from static timing analysis," in *International Symposium on Quality Electronic Design*, pp. 437–442, 2001.

[63] G. Gielen and R. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proceedings of the IEEE*, vol. 88, no. 12, pp. 1825–1854, 2000.

[64] G. Gielen, H. Walscharts, and W. Sansen, "Analog circuit design optimization based on symbolic simulation and simulated annealing," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 3, pp. 707–713, 1990.

[65] P. Gupta, A. Kahng, A. Kasibhatla, and P. Sharma, "Eyecharts: Constructive benchmarking of gate sizing heuristics," in *Proceedings of Design Automation Conference*, 2010.

[66] P. Gupta, A. Kahng, P. Sharma, and D. Sylvester, "Gate-length biasing for runtime-leakage control," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 8, pp. 1475–1485, 2006.

[67] P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, "Selective gate-length biasing for cost-effective runtime leakage control," in *Proceedings of Design Automation Conference*, pp. 327–330, 2004.

[68] R. Gupta, B. Tutuianu, and L. Pileggi, "The Elmore delay as a bound for RC trees with generalized input signals," *IEEE Transactions on Computer-Aided Design*, vol. 16, no. 1, pp. 95–104, 1997.

[69] M. Guthaus, N. Venkateswaran, C. Visweswariah, and V. Zolotov, "Gate sizing using incremental parameterized statistical timing analysis," in *Proceedings of International Conference on Computer-Aided Design*, pp. 1029–1036, 2005.

[70] R. Haddad, L. van Ginneken, and N. Shenoy, "Discrete drive selection for continuous sizing," in *Proceedings of International Conference on Computer Design*, pp. 110–115, October 1997.

[71] M. Hansen, H. Yalcin, and J. Hayes, "Unveiling the ISCAS-85 benchmarks: A case study in reverse engineering," *IEEE Design and Test*, vol. 16, pp. 72–80, July–September 1999.

[72] R. Harjani, R. Rutenbar, and L. Carley, "OASYS: A framework for analog circuit synthesis," *IEEE Transactions on Computer-Aided Design*, vol. 8, no. 12, pp. 1247–1266, 1989.

Full text available at: http://dx.doi.org/10.1561/1000000019

[73] M. Hashimoto and H. Onodera, "Post-layout transistor sizing for power reduction in cell-based design," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 359–365, 2001.

[74] S. Held, "Gate sizing for large cell-based designs," in *Proceedings of the Conference on Design, Automation and Test in Europe* (3001 Leuven, Belgium, Belgium), pp. 827–832, 2009.

[75] M. Hershenson, S. Boyd, and T. Lee, "Optimal design of a CMOS op-amp via geometric programming," *IEEE Transactions on Computer-Aided Design*, vol. 20, no. 1, pp. 1–21, 2001.

[76] S. Hu, M. Ketkar, and J. Hu, "Gate sizing for cell library-based designs," in *Proceedings of Design Automation Conference*, pp. 847–852, 2007.

[77] S. Hu, M. Ketkar, and J. Hu, "Gate sizing for cell-library-based designs," *IEEE Transactions on Computer-Aided Design*, vol. 28, no. 6, pp. 818–825, 2009.

[78] Y. Huang, J. Hu, and W. Shi, "Lagrangian relaxation for gate implementation selection," in *Proceedings of International Conference on Physical Design*, pp. 167–174, 2011.

[79] International Technology Roadmap for Semiconductors — Design Available on http://www.itrs.net.

[80] K. Jeong and A. Kahng, "Methodology from chaos in ic implementation," in *Proceedings of International Conference on Quality Electronic Design*, pp. 885–892, 2010.

[81] A. Kahng, B. Liu, and X. Xu, "Constructing current-based gate models based on existing timing library," in *Proceedings of the International Symposium on Quality Electronic Design*, pp. 37–42, 2006.

[82] T. Karnik, Y. Ye, J. Tschanz, L. Wei, S. Burns, V. Govindarajulu, V. De, and S. Borkar, "Total power optimization by simultaneous dual-vt allocation and device sizing in high performance microprocessors," in *Proceedings of Design Automation Conference*, pp. 486–491, 2002.

[83] K. Kasamsetty, M. Ketkar, and S. Sapatnekar, "A new class of convex functions for delay modeling and its application to the transistor sizing problem [cmos gates]," *IEEE Transactions on Computer-Aided Design*, vol. 19, no. 7, pp. 779–788, 2000.

[84] I. Keller, K. Tam, and V. Kariat, "Challenges in gate level modeling for delay and SI at 65 nm and below," in *Proceedings of Design Automation Conference*, pp. 468–473, 2008.

[85] V. Khandelwal and A. Srivastava, "A general framework for accurate statistical timing analysis considering correlations," in *Proceedings of Design Automation Conference*, pp. 89–94, 2005.

[86] T. I. Kirkpatrick and N. R. Clark, "Pert as an aid to logic design," *IBM Journal of Research and Development*, vol. 10, pp. 135–141, March 1966.

[87] H. Koh, C. Sequin, and P. Gray, "OPASYN: A compiler for CMOS operational amplifiers," *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 2, pp. 113–125, 1990.

[88] M. Krasnicki, R. Phelps, R. A. Rutenbar, and L. R. Carley, "Maelstrom: Efficient simulation-based synthesis for custom analog cells," in *Proceedings of Design Automation Conference*, pp. 945–950, 1999.

Full text available at: http://dx.doi.org/10.1561/1000000019

[89] J. Lee and P. Gupta, "Incremental gate sizing for late process changes," in *Proceedings of International Conference on Computer Design*, pp. 215–221, October 2010.

[90] J.-F. Lee and D. T. Tang, "An algorithm for incremental timing analysis," in *Proceedings of Design Automation Conference*, pp. 696–701, 1995.

[91] C. Lemaréchal, "Lagrangian relaxation," *Computational Combinatorial Optimization*, pp. 112–156, 2001.

[92] W. Li, "Strongly np-hard discrete gate sizing problems," in *Proceedings of International Conference on Computer Design*, pp. 468–471, October 1993.

[93] X. Li, J. Le, and L. Pileggi, "Statistical performance modeling and optimization," *Foundations and Trends® in Electronic Design Automation*, vol. 1, no. 4, pp. 331–480, 2006.

[94] X. Li, J. Le, and L. T. Pileggi, *Statistical Performance Modeling and Optimization*. Hanover, MA, USA: Now Publishers Inc., 2007.

[95] C. Liao and S. Hu, "Approximation scheme for restricted discrete gate sizing targeting delay minimization," *Journal of Combinatorial Optimization*, vol. 21, no. 4, pp. 497–510, 2011.

[96] H.-R. Lin and T.-T. Hwang, "Power reduction by gate sizing with path-oriented slack calculation," in *Proceedings of Asia and South Pacific Design Automation Conference*, 1995.

[97] R. Lin and M. Wu, "A new statistical approach to timing analysis of vlsi circuits," in *Proceedings of International Conference on VLSI Design*, pp. 507–513, 1998.

[98] S. Lin, M. Marek-Sadowska, and E. Kuh, "Delay and area optimization in standard-cell design," *Proceedings of Design Automation Conference*, pp. 349–352, June 1990.

[99] J.-J. Liou, A. Krstic, L.-C. Wang, and K.-T. Cheng, "False-path-aware statistical timing analysis and efficient path selection for delay testing and timing validation," in *Proceedings of Design Automation Conference*, pp. 566–569, 2002.

[100] Y. Liu and J. Hu, "A new algorithm for simultaneous gate sizing and threshold voltage assignment," in *Proceedings of International Conference on Physical Design*, pp. 27–34, 2009.

[101] Y. Liu and J. Hu, "A new algorithm for simultaneous gate sizing and threshold voltage assignment," *IEEE Transactions on Computer-Aided Design*, vol. 29, pp. 223–234, February 2010.

[102] R. Macys and S. McCormick, "A new algorithm for computing the effective capacitance in deep sub-micron circuits," in *Proceedings of the Custom Integrated Circuits Conference*, pp. 313–316, 1998.

[103] H. Mangassarian and M. Anis, "On statistical timing analysis with inter-and intra-die variations," in *Proceedings of the Conference on Design, Automation and Test in Europe-Volume 1*, pp. 132–137, 2005.

[104] M. Mani, A. Devgan, and M. Orshansky, "An efficient algorithm for statistical minimization of total power under timing yield constraints," in *Proceedings of Design Automation Conference*, pp. 309–314, 2005.

Full text available at: http://dx.doi.org/10.1561/1000000019

[105] M. Mani, A. Devgan, M. Orshansky, and Y. Zhan, "A statistical algorithm for power- and timing-limited parametric yield optimization of large integrated circuits," *IEEE Transactions on Computer-Aided Design*, vol. 26, pp. 1790–1802, October 2007.

[106] M. Mani and M. Orshansky, "A new statistical optimization algorithm for gate sizing," in *Proceedings of IEEE International Conference on Computer Design*, pp. 272–277, 2004.

[107] T. Massier, H. Graeb, and U. Schlichtmann, "The sizing rules method for CMOS and bipolar analog integrated circuit synthesis," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 12, pp. 2209–2222, 2008.

[108] T. McConaghy, P. Palmers, G. Gielen, and M. Steyaert, "Automated extraction of expert knowledge in analog topology selection and sizing," 2008.

[109] S. Mok, "Post-layout sizing for leakage power optimization: A comparative study," Master's Thesis, Department of Electrical Engineering, University of California at Los Angeles, 2010.

[110] S. Mok, "Propagation delay approximation considering effective capacitance and slew degradation," Techical Report, UCLA, Available on http://nanocad.ee.ucla.edu/pub/Main/Publications/MSTR4_paper.pdf, 2011.

[111] F. N. Najm, "On the need for statistical timing analysis," in *Proceedings of Design Automation Conference*, pp. 764–765, 2005.

[112] G. Nam, "Ispd 2006 placement contest: Benchmark suite and results," in *Proceedings of International Conference on Physical Design*, pp. 167–167, 2006.

[113] G. Nam, M. Yildiz, D. Pan, and P. Madden, "Ispd placement contest updates and ispd 2007 global routing contest," in *Proceedings of International Conference on Physical Design*, pp. 167–167, 2007.

[114] Nangate Open Cell Library v1.3 Available on http://www.si2.org/openeda.si2.org/projects/nangatelib.

[115] S. Narendra, "Challenges and design choices in nanoscale CMOS," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 1, no. 1, pp. 7–49, 2005.

[116] S. Nassif, A. Strojwas, and S. Director, "A methodology for worst-case analysis of integrated circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 5, no. 1, pp. 104–113, January 1986.

[117] D. Nguyen, A. Davare, M. Orshansky, D. Chinnery, B. Thompson, and K. Keutzer, "Minimization of dynamic and static power through joint assignment of threshold voltages and sizing optimization," in *Proceedings of International Conference on Low Power Electronics and Design*, pp. 158–163, 2003.

[118] W. Nye, D. Riley, A. Sangiovanni-Vincentelli, and A. Tits, "DELIGHT. SPICE: An optimization-based system for the design of integrated circuits," *IEEE Transactions on Computer-Aided Design*, vol. 7, no. 4, pp. 501–519, 1988.

[119] E. Ochotta, R. Rutenbar, and L. Carley, "Synthesis of high-performance analog circuits in ASTRX/OBLX," *IEEE Transactions on Computer-Aided Design*, vol. 15, no. 3, pp. 273–294, 1996.

Full text available at: http://dx.doi.org/10.1561/1000000019

[120] M. Orshansky and K. Keutzer, "A general probabilistic framework for worst case timing analysis," in *Proceedings of Design Automation Conference*, pp. 556–561, 2002.

[121] M. Ozdal, S. Burns, and J. Hu, "Gate sizing and device technology selection algorithms for high-performance industrial designs," in *Proceedings of International Conference on Computer-Aided Design*, pp. 724–731, November 2011.

[122] P. Pant, V. De, and A. Chatterjee, "Simultaneous power supply, threshold voltage, and transistor size optimization for low-power operation of cmos circuits," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 6, no. 4, pp. 538–545, 1998.

[123] P. Pant, R. Roy, and A. Chattejee, "Dual-threshold voltage assignment with transistor sizing for low power cmos circuits," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 9, no. 2, pp. 390–394, 2001.

[124] D. Patil, S. Yun, S. Kim, A. Cheung, M. Horowitz, and S. Boyd, "A new method for design of robust digital circuits," in *Proceedings of International Conference on Quality Electronic Design*, pp. 676–681, 2005.

[125] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of mos transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[126] R. Phelps, M. Krasnicki, R. Rutenbar, L. Carley, and J. Hellums, "ANACONDA: Robust synthesis of analog circuits via stochastic pattern search," in *Proceedings of Custom Integrated Circuits*, pp. 567–570, 1999.

[127] L. Pillage and R. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 4, pp. 352–366, 1990.

[128] J. Qian, S. Pullela, and L. Pillage, "Modeling the effective capacitance for the RC interconnect of CMOS gates," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 12, pp. 1526–1535, 1994.

[129] A. Ramalingam, A. Singh, S. Nassif, G. Nam, M. Orshansky, and D. Pan, "An accurate sparse-matrix based framework for statistical static timing analysis," *Integration, the VLSI Journal*, 2011.

[130] R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, "Statistical analysis of subthreshold leakage current for VLSI circuits," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 12, no. 2, pp. 131–139, 2004.

[131] D. Rautenbach and C. Szegedy, "A class of problems for which cyclic relaxation converges linearly," *Computational Optimization and Applications*, vol. 41, no. 1, pp. 53–60, 2008.

[132] S. Roy, W. C. aad C. Chen, and Y. Hu, "Numerically convex forms and their application in gate sizing," *IEEE Transactions on Computer-Aided Design*, vol. 26, no. 9, pp. 1637–1647, 2007.

[133] S. Roy and W. Chen, "Convexfit: An optimal minimum-error convex fitting and smoothing algorithm with application to gate-sizing," in *Proceedings of International Conference on Computer-Aided Design*, pp. 196–203, 2005.

[134] S. Roy, Y. H. Hu, C. C.-P. Chen, S.-P. Hung, T.-Y. Chiang, and J.-G. Tseng, "An optimal algorithm for sizing sequential circuits for industrial library based

Full text available at: http://dx.doi.org/10.1561/1000000019

designs," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 148–151, 2008.

[135] A. Ruehli, P. Wolff, and G. Goertzel, "Analytical power/timing optimization technique for digital system," in *Proceedings of Design Automation Conference*, pp. 142–146, 1977.

[136] T. Sakurai and A. Newton, "Alpha-power law mosfet model and its applications to cmos inverter delay and other formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 584–594, April 1990.

[137] S. Sapatnekar, *Timing*. Springer, Netherlands, 2004.

[138] S. Sapatnekar and W. Chuang, "Power vs. delay in gate sizing: Conflicting objectives?," in *Proceedings of International Conference on Computer-Aided Design*, pp. 463–466, November 1995.

[139] N. Satish, K. Ravindran, M. Moskewicz, D. Chinnery, and K. Keutzer, "Evaluating the effectiveness of statistical gate sizing for power optimization," Technical Report, University of California at Berkeley, ERL Memorandum M05/28, August 2005.

[140] C. Sechen and H. Tennakoon, "Gate sizing using lagrangian relaxation combined with a fast gradient-based pre-processing step," in *Proceedings of International Conference on Computer-Aided Design*, pp. 395–402, 2002.

[141] S. Shah, A. Srivastava, D. Sharma, D. Sylvester, D. Blaauw, and V. Zolotov, "Discrete vt assignment and gate sizing using a self-snapping continuous formulation," in *Proceedings of International Conference on Computer-Aided Design*, pp. 705–712, 2005.

[142] B. Sheu, D. Scharfetter, P. Ko, and M. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 558–566, 1987.

[143] J. Shyu, A. Sangiovanni-Vincentelli, J. Fishburn, and A. Dunlop, "Optimization-based transistor sizing," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 2, pp. 400–409, 1988.

[144] L. Silveira, M. Kamon, J. White, and I. Elfadel, "A coordinate-transformed Arnoldi algorithm for generating guaranteed stable reduced-order models of RLC circuits," in *Proceedings of International Conference on Computer-Aided Design*, p. 288, 1996.

[145] J. Singh, Z.-Q. Luo, and S. Sapatnekar, "A geometric programming-based worst case gate sizing method incorporating spatial correlation," *IEEE Transactions on Computer-Aided Design*, vol. 27, pp. 295–308, February 2008.

[146] J. Singh, V. Nookala, Z. Luo, and S. Sapatnekar, "Robust gate sizing by geometric programming," in *Proceedings of Design Automation Conference*, pp. 315–320, 2005.

[147] J. Singh and S. Sapatnekar, "Statistical timing analysis with correlated non-Gaussian parameters using independent component analysis," in *Proceedings of Design Automation Conference*, pp. 155–160, 2006.

[148] S. Sirichotiyakul, T. Edwards, C. Oh, R. Panda, and D. Blaauw, "Duet: An accurate leakage estimation and optimization tool for dual-Vt circuits," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 10, no. 2, pp. 79–90, 2002.

Full text available at: http://dx.doi.org/10.1561/1000000019

[149] S. Sirichotiyakul, T. Edwards, C. Oh, J. Zuo, A. Dharchoudhury, R. Panda, and D. Blaauw, "Stand-by power minimization through simultaneous threshold voltage selection and circuit sizing," in *Proceedings of Design Automation Conference*, pp. 436–441, 1999.

[150] A. Srivastava, D. Sylvester, and D. Blaauw, "Power minimization using simultaneous gate sizing, dual-vdd and dual-vth assignment," in *Proceedings of Design Automation Conference*, pp. 783–787, 2004.

[151] A. Srivastava, D. Sylvester, and D. Blaauw, "Statistical optimization of leakage power considering process variations using dual-Vth and sizing," in *Proceedings of Design Automation Conference*, pp. 773–778, 2004.

[152] A. Srivastava, D. Sylvester, and D. Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*. Springer Verlag, 2005.

[153] V. Stojanovic, D. Markovic, B. Nikolic, M. Horowitz, and R. Brodersen, "Energy–delay tradeoffs in combinational logic using gate sizing and supply voltage optimization," in *Proceedings of European Solid-State Circuits Conference (ESSCIRC)*, pp. 211–214, 2005.

[154] I. Sutherland and R. Sproull, "Logical effort: Designing for speed on the back of an envelope," in *Proceedings of the 1991 University of California/Santa Cruz Conference on Advanced Research in VLSI*, pp. 1–16, 1991.

[155] I. Sutherland, R. Sproull, and D. Harris, *Logical Effort: Designing Fast CMOS Circuits*. Morgan Kaufmann, 1999.

[156] Synopsys, "Liberty open source library modeling," Web resource, http://www.opensourceliberty.org.

[157] Synopsys, "NanoTime," http://www.synopsys.org.

[158] Y. Tamiya, Y. Matsunaga, and M. Fujita, "Lp based cell selection with constraints of timing, area, and power consumption," in *Proceedings of International Conference on Computer-Aided Design*, pp. 378–381, 1994.

[159] T. Tokuda, J. Korematsu, O. Tomisawa, S. Asai, I. Ohkura, and T. Enomoto, "A hierarchical standard cell approach for custom VLSI design," *IEEE Transactions on Computer-Aided Design*, vol. 3, no. 3, pp. 172–177, 1984.

[160] R. Trihy, "Addressing library creation challenges from recent liberty extensions," in *Proceedings of Design Automation Conference*, pp. 474–479, 2008.

[161] S. Tsukiyama, M. Tanaka, and M. Fukui, "A statistical static timing analysis considering correlations between delays," in *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 353–358, 2001.

[162] P. Tuohy, A. Gribben, A. Walton, , and J. Robertson, "Realistic worst-case parameters for circuit simulation," in *Proceedings of Communications, Speech and Vision*, pp. 137–140, 1987.

[163] V. Veetil, D. Sylvester, and D. Blaauw, "A lower bound computation method for evaluation of statistical design techniques," in *Proceedings of International Conference on Computer-Aided Design*, pp. 562–569, 2010.

[164] C. Visweswariah, "Death, taxes and failing chips," in *Proceedings of Design Automation Conference*, pp. 343–347, 2003.

[165] C. Visweswariah, K. Ravindran, K. Kalafala, S. Walker, and S. Narayan, "First-order incremental block-based statistical timing analysis," in *Proceedings of Design Automation Conference*, pp. 331–336, 2004.

Full text available at: http://dx.doi.org/10.1561/1000000019

[166] J. Wang, D. Das, and H. Zhou, "Gate sizing by lagrangian relaxation revisited," *IEEE Transactions on Computer-Aided Design*, vol. 28, no. 7, pp. 1071–1084, 2009.

[167] Q. Wang and S. Vrudhula, "Static power optimization of deep submicron cmos circuits for dual vt technology," in *Proceedings of International Conference on Computer-Aided Design*, pp. 490–496, 1998.

[168] L. Wei, K. Roy, and C. Koh, "Power minimization by simultaneous dual-Vth assignment and gate-sizing," in *Proceedings of the Custom Integrated Circuits Conference*, pp. 413–416, 2000.

[169] T. Wu and A. Davoodi, "PaRS: Parallel and near-optimal grid-based cell sizing for library-based design," *IEEE Transactions on Computer-Aided Design*, vol. 28, no. 11, pp. 1666–1678, 2009.

[170] T. Xiao and M. Marek-Sadowska, "Gate sizing to eliminate crosstalk induced timing violation," in *Proceedings of the International Conference on Computer Design*, p. 0186, 2001.

[171] Y. Zhan, A. Strojwas, X. Li, L. Pileggi, D. Newmark, and M. Sharma, "Correlation-aware statistical timing analysis with non-Gaussian delay distributions," in *Proceedings of Design Automation Conference*, pp. 77–82, 2005.

[172] L. Zhang, W. Chen, Y. Hu, J. Gubner, and C. Chen, "Correlation-preserved non-Gaussian statistical timing analysis with quadratic timing model," in *Proceedings of Design Automation Conference*, pp. 83–88, 2005.

[173] L. Zhang, Y. Hu, and C. Chen, "Statistical timing analysis with path reconvergence and spatial correlations," in *Proceedings of Design, Automation and Test in Europe*, p. 112, 2006.

[174] Q. Zhou and K. Mohanram, "Gate sizing to radiation harden combinational logic," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 1, pp. 155–166, 2006.

[175] C. Zhuo, D. Blaauw, and D. Sylvester, "Variation-aware gate sizing and clustering for post-silicon optimized circuits," in *Proceedings of the International Conference on Low Power Electronics and Design*, pp. 105–110, 2008.