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Abstract

With greater integration, the power dissipation in integrated circuits has begun to outpace the ability of today's heat sinks to limit the on-chip temperature. As a result, thermal issues have come to the forefront, and thermally aware design techniques are likely to play a major role in the future. While improved heat sink technologies are available, economic considerations restrict them from being widely deployed until and unless they become more cost-effective. Low power design is helpful in controlling on-chip temperatures, but is already widely utilized, and new thermal-specific approaches are necessary. In short, the onus on thermal management is beginning to move from the package designer toward the chip designer. This survey provides an overview of analysis and optimization techniques for thermally aware design. After beginning with a motivation for the problem and trends seen in the semiconductor industry, the survey presents a description

of techniques for on-chip thermal analysis. Next, the effects of elevated temperatures on on-chip performance metrics are analyzed. Finally, a set of thermal optimization techniques, for controlling on-chip temperatures and limiting the level to which they degrade circuit performance, are described.

Contents

1

Introduction

1.1 Overview

Thermal analysis is important in ensuring the accuracy of timing, noise, and reliability analyses during chip design. The thermal properties of integrated systems can be studied at a number of levels and length scales, as partly illustrated in Figure 1.1. For the problem of cooling racks of computing servers in a data center, the cooling structure must cover an area of the order of meter to tens of meters. At the next level, board-level cooling operates at length scales of the order of a tenth of a meter, while package level cooling corresponds to lengths of the order of centimeters. Within-chip solutions include microrefrigeration solutions, whose sizes range from the order of a millimeter to a centimeter [132] and can operate at the architectural level, to solutions that can scale down to several tens of microns [131] and operate at about the logic level.

In other words, the thermal problem is important at a wide range of length scales, and known cooling solutions exist at all of these levels. These solutions range in complexity and cost from the use of passive heat sinks, to active convective cooling using fans, to more exotic

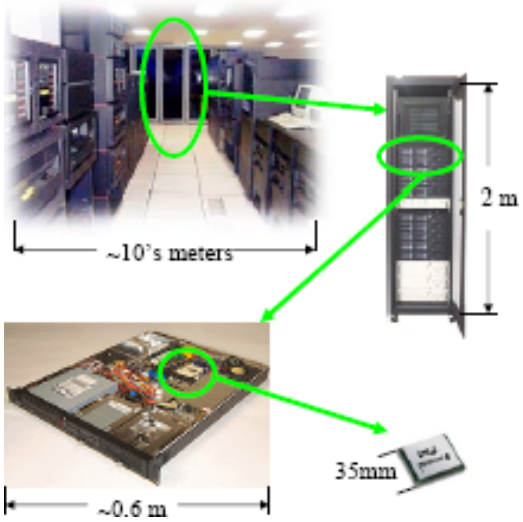

Fig. 1.1 Manifestations of the thermal problem at a variety of length scales [72] ©Therminic reprinted with permission.

technologies based on microchannels and microrefrigeration. Some of these solutions are more traditional and have been available, in some form, for quite a few years, while others are relatively newer, and are actively being researched.

The genesis of thermal problems is in the fact that electronic circuitry dissipates power. This power dissipated on-chip is manifested in the form of heat, which, in a reasonably designed system, flows toward a heat sink. The power generated per unit area is often referred to as the heat flux. Temperature and power (or heat flux) are intimately related, but it is important to note that they are distinct from each other. For instance:

- For the same total power, it is possible to build systems with different peak temperature and heat flux distributions, simply by changing the spatial arrangement of the power sources. If all the high power sources are concentrated together in a region, that area will probably see a high peak temperature. Such a thermal bottleneck can often be relieved by moving the power sources apart.

- The relative location of the power sources to the heat sink also plays a part in determining the on-chip temperature, and by providing high-power elements with a conductive path to the heat sink, many thermal problems can be alleviated.

Most such optimizations can result in tradeoffs: for instance, thermal considerations imply that highly active units should be moved apart, but if these units communicate with each other, performance requirements may dictate that they be kept close to each other.

The focus of this survey is on presenting solutions for the within-chip thermal problem. However, an essential prerequisite to addressing thermal issues is the ability to model heat transfer paths of a chip with its surrounding environment, and to analyze the entire thermal system, including effects that are not entirely within the chip. Figure 1.1 shows a representative chip in a ceramic ball grid array (CBGA) packaging and its surrounding environment. This is modeled as a network of thermal resistors, using the thermal–electrical analogy to be described in Section 2.3.1, where power values map on to electrical currents, temperatures to voltages, and the ground node to the ambient.

In Figure 1.2, the chip is placed over a ceramic substrate, connected through flip-chip, or C4, connections all over its area. The substrate is connected to the printed circuit board through CBGA connections, and a small portion of the heat generated on-chip flows through this region to the ambient, which is denoted by the ground connection in the thermal circuit. At the other end, a heat sink with a large surface area is connected to the chip, with a thermal interface material lying between the chip and the heat sink. The role of the thermal interface material (TIM) is to act as a heat spreader. In the absence of this material, the surface roughness of the chip and the heat sink imply that the actual contact between the two surfaces could be as low as 1%–2% of the apparent surface area [111], and this is accentuated by warpage of the die under thermal stress; adding that the TIM improves the contact area, and consequently, the thermal resistance at this interface. The upper half of the thermal circuit shows how this region can be modeled.

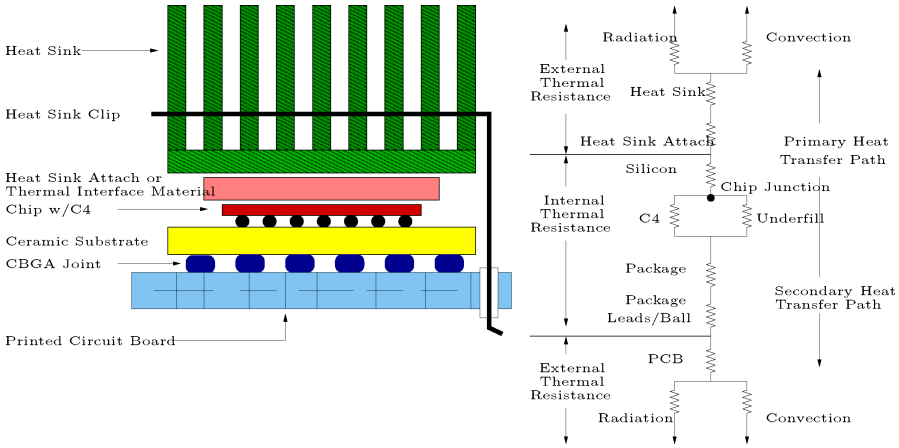

Fig. 1.2 Heat dissipation paths of a chip in a system [142] ©IEEE reprinted with permission.

Additional air-cooling schemes, such as fans that are connected to the heat sink, can be incorporated into this model.

A crucial step in design involves the choice of a heat sink: here, approximate techniques may be used to obtain a reasonable sinking solution [89], based on a gross characterization of the sink by its thermal resistance. At the package design level, a key item of interest is the thermal design power (TDP), which is the maximum sustained power dissipated by an integrated circuit. This is not necessarily the peak power: if the peak power is dissipated for a small period of time that is below the thermal time constant, it does not appreciably affect the choice of the heat sink. If the peak temperature is to be maintained at a temperature T_{peak} above the ambient temperature, then the maximum thermal resistance of the heat sink is given by a simple formula based on a lumped DC analysis:

$$R_{\text{sink}} = T_{\text{peak}}/\text{TDP}. \tag{1.1}$$

The choice of the heat sink can be made on the basis of this requirement. Note that this is a very coarse analysis that does not consider transient effects.

1.2 Thermal Trends

1.2.1 The Importance of Temperature as a Design Consideration

The problem of getting the heat out of a chip is not new: indeed, power issues have been at least partially if not wholly responsible for the demise of a variety of technologies before CMOS. For instance, as demonstrated in Figure 1.3, the rapidly increasing power dissipation trends in bipolar circuits played a large role in their displacement as the dominant technology of the day, being taken over first by NMOS and then by CMOS. Today, no clear successor to CMOS has emerged, but on-chip power dissipation has emerged as a major design bottleneck, and it is ever more important to build cooling solutions from the system level down to the subchip level. Historical trends, illustrated in Figure 1.3, show an ever-increasing profile for the volume of the external heat sink as on-chip power goes up, and this is unsustainable.

As illustrated in Figure 1.4, trends show that the cost of the cooling solution is a nonlinear function of the chip power dissipation: the initial rise is gentle, but beyond the point of convective cooling, the costs rise

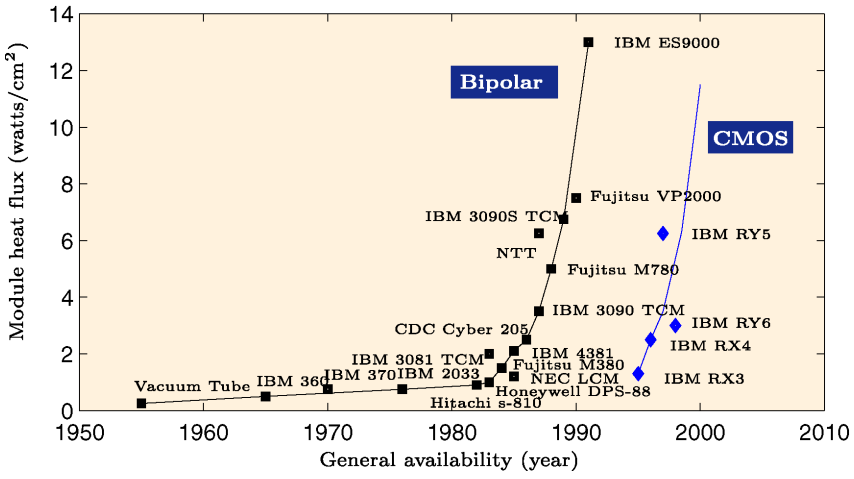

Fig. 1.3 Trends for the heat flux for state-of-the-art systems over the years [27] ©IEEE reprinted with permission.

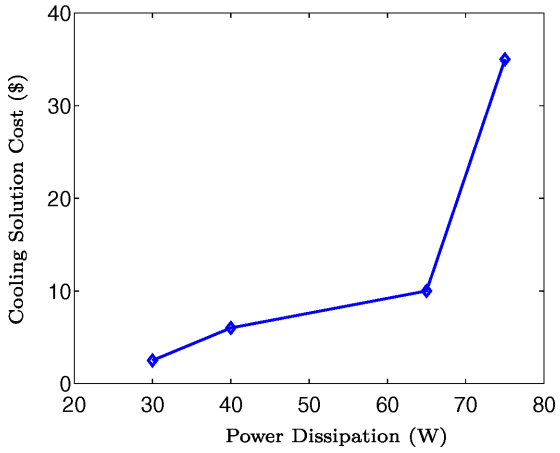

Fig. 1.4 Cooling costs as a function of the power dissipation [55] ©Intel Technology Journal reprinted with permission.

steeply. This knee point is a function of cooling system complexity and the volume of actively cooled packages/technologies, and may arguably permit slightly higher on-chip power dissipation in the future as newer technologies gain economies of scale, but the fundamental nature of the curve — of having a gentle ascent followed by a steep rise beyond a knee point — is unlikely to change. This has consequences on the size of the heat sink, and Figure 1.5 shows how the volume of the heat sink has increased with increased on-chip power.

To achieve the required heat sinking solution, it may be necessary to increase the heat sink size to unreasonable levels, or to move to new cooling technologies. For contemporary high-end, large-volume parts, anything that is more complex than air-cooling is probably too expensive. Although several of the bipolar chips in Figure 1.3, after 1980, used some form of water cooling [27], liquid cooling is not seen as a very viable solution today. There have been numerous improvements even in air-cooled technologies and improved thermal interface materials in the recent past, which have progressively shifted the knee of the cooling cost curve of Figure 1.4 progressively to the right, so that the heat fluxes that are currently obtained by air cooling could only be achieved by liquid cooling in the 1980s [122]. However, even these

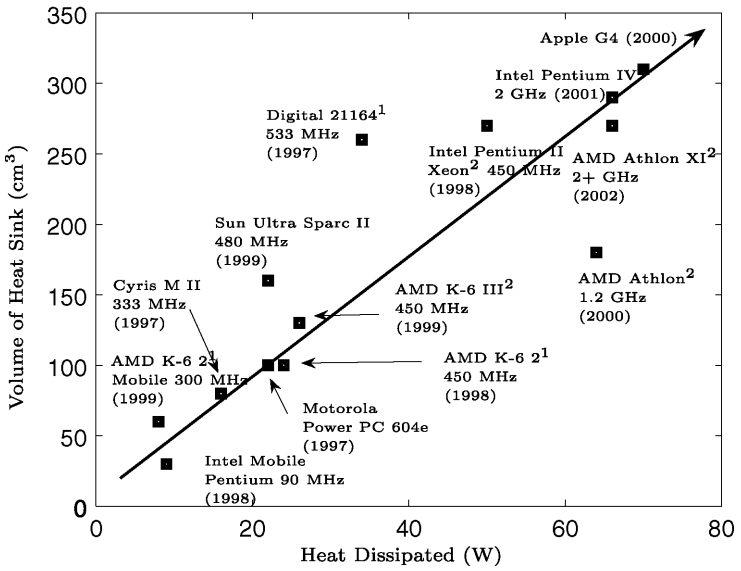

Fig. 1.5 Historical data showing the volume of the heat sink as a function of the total on-chip power [72].

improvements cannot keep up with the capability of Moore's law to integrate more functionality on a chip. Indeed, while it is possible to pack more transistors on a chip today, only a fraction of them can actually be used to full potential, because of power and thermal limitations. More advanced solutions using, for example microfluidic channels and microrefrigeration, have been proposed, these are not cost-effective enough for widespread use today.

1.2.2 Thermal Issues in 3D Integrated Circuits

The previous subsection explains why temperature must be an important consideration in the design of nanoscale integrated circuits. A further motivator for thermally conscious design has come about with the advent of three dimensional (3D) integration, which makes the on-chip problem particularly acute.

Unlike conventional 2D circuits, where all transistors are placed in a single plane, with several layers of interconnect above, 3D circuits stack tiers of such 2D structures, one above the other. 3D structures may be

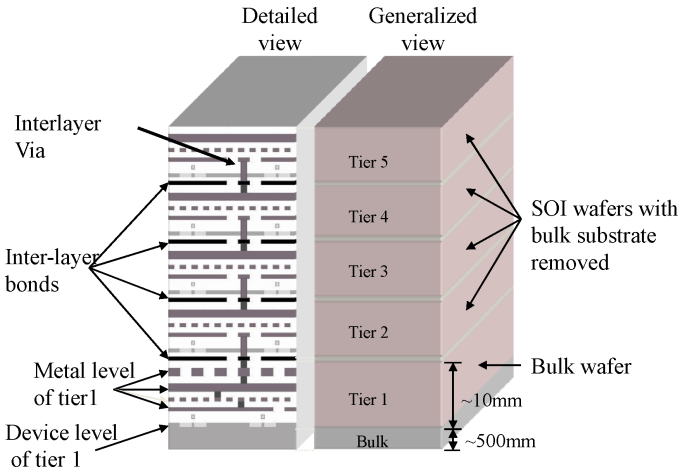

Fig. 1.6 A schematic of a 3D integrated circuit.

built by stacking tiers of dies above each other, where the separation between tiers equals the thickness of the bulk substrate, which is of the order of several hundreds of microns. Advances in industrial [54], government [18], and academic [119] research laboratories have demonstrated 3D designs with inter-tier separations of the order of a few microns, enabling short connections between tiers, accentuating the advantages of short vertical interconnections in these 3D structures. A schematic of a 3D chip is illustrated in Figure 1.6, showing five tiers stacked over each other. The lowest tier sits over a bulk substrate, while the other tiers are thinned to remove the substrate, and provide inter-tier distances of the order of ten microns.

With these technological advances, 3D technologies provide a roadmap for allowing increased levels of integration within the same footprint, in a direction that is orthogonal to Moore's law. Moreover, 3D technologies provide the ability to locate critical blocks close to each other, e.g., by placing memory units in close proximity to processors by placing them one above the other. These, and other, advantages make 3D a promising technology for the near future.

However, the increased packing density afforded by 3D integration has the drawback of exacerbating thermal issues. Based on a simple

back-of-the-envelope calculation, a k-tier 3D chip could use k times as much current as a single 2D chip of the same footprint; however, the packaging technology is not appreciably different. This implies that the corresponding heat generated must be sent out to the environment using a package with essentially similar heat sinking capabilities. As a result, the on-chip temperature on a 3D chip could be k times higher than the 2D chip. While this is a very coarse analysis with very coarse assumptions, the eventual conclusion — that thermal effects are a major concern in 3D circuits — is certainly a strong motivator for paying increased attention to thermal issues today.

1.3 Organization of the Survey

This survey begins its discussion of on-chip thermal effects by surveying techniques for evaluating the distribution of temperature on a chip. These analysis techniques essentially solve a partial differential equation (PDE) that relates the power dissipated on a chip to its temperature profile. While the solution of PDEs is a well-studied problem, it is possible to take advantage of some specific properties of the on-chip problem to obtain an efficient solution. Moreover, thermal analysis shows similarities to other well-studied problems in integrated circuit design, most notably, those of analyzing on-chip power grids [128], and of substrate analysis [46, 36], and techniques from these domains can be borrowed to enhance the quality of algorithms for thermal analysis.

Next, we study the manner in which on-chip temperatures affect the properties and performance of a circuit. In terms of delay, the performance of transistors and the resistance of interconnect wires can be affected; in terms of power dissipation, there is a strong relationship, with potential feedback, between temperature and leakage power; in terms of reliability, the lifetime of both devices and interconnects all depend critically on the operating temperature of the circuit. These are all critical factors in ensuring circuit performance, and the complexity of these problems makes it essential to build efficient and scalable CAD solutions for on-chip thermal analysis. Finally, we overview some representative techniques for thermally driven circuit optimization.

References

[1] "HotSpot," available at: http://lava.cs.virginia.edu/HotSpot/index.htm.

[2] C. Ababei, Y. Feng, B. Goplen, H. Mogal, T. Zhang, K. Bazargan, and S. Sapatnekar, "Placement and routing in 3D integrated circuits," *IEEE Design and Test*, vol. 22, no. 6, pp. 520–531, November–December 2005.

[3] A. H. Ajami, K. Banerjee, and M. Pedram, "Analysis of substrate thermal gradient effects on optimal buffer insertion," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 44–48, 2001.

[4] A. H. Ajami, K. Banerjee, and M. Pedram, "Modeling and analysis of nonuniform substrate temperature effects on global ULSI interconnects," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 24, no. 6, pp. 849–861, June 2005.

[5] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for pMOSFETs," in *IEEE International Electronic Devices Meeting*, pp. 14.4.1–14.4.4, 2003.

[6] M. A. Alam, "On the reliability of micro-electronic devices: An introductory lecture on negative bias temperature instability," Nanotechnology 501 Lecture Series; available at http://www.nanohub.org/resources/?id=193, 2005.

[7] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Journal of Microelectronics Reliability*, vol. 45, pp. 71–81, August 2004.

[8] A. Andrei, M. Schmitz, P. Eles, Z. Peng, and B. M. Al-Hashimi, "Overhead-conscious voltage selection for dynamic and leakage energy reduction of time-constrained systems," in *Proceedings of the Design, Automation and Test in Europe*, pp. 518–523, 2004.

[9] K. Banerjee and A. Mehrotra, "Global (interconnect) warming," *IEEE Circuits and Devices*, pp. 16–32, September 2001.

[10] P. Bannon, "Alpha 21364: A scalable single-chip SMP," available at: http://www.digital.com/alphaoem/micro- processorforum.htm, 1998.

[11] W. Batty, C. E. Christoffersen, A. J. Panks, S. David, C. M. Snowden, and M. B. Steer, "Electrothermal CAD of power devices and circuits with fully physical time-dependent compact thermal modeling of complex nonlinear 3-D systems," *IEEE Transactions on Components and Packaging Technologies*, vol. 34, no. 4, pp. 566–590, December 2001.

[12] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive modeling of the NBTI effect for reliable design," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 189–192, 2006.

[13] J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," in *Proceedings of the IEEE*, vol. 57, pp. 1587–1594, September 1969.

[14] K. Bowman, L. Wang, X. Tang, and J. Meindl, "A circuit-level perspective of the optimum gate oxide thickness," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1800–1810, August 2001.

[15] W. L. Briggs, "A multigrid tutorial," http://www.llnl.gov/CASC/people/henson/mgtut/ps/mgtut.pdf.

[16] D. Brooks, V. Tiwari, and M. Martonosi, "Wattch: A framework for architectural-level power analysis and optimization," in *Proceedings of the ACM International Symposium on Computer Architecture*, pp. 83–94, 2000.

[17] D. C. Burger and T. M. Austin, "The SimpleScalar tool set, version 2.0," Technical Report CS-TR-97-1342, The University of Wisconsin, Madison, June 1997.

[18] J. Burns, L. McIlrath, J. Hopwood, C. Keast, D. P. Vu, K.Warner, and P. Wyatt, "An SOI-based three dimensional integrated circuit technology," in *Proceedings of the IEEE International SOI Conference*, pp. 20–21, 2000.

[19] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. Machala, and S. Krishnan, "A comprehensive framework for predictive modeling of negative bias temperature instability," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 273–282, 2004.

[20] H. Chang and S. S. Sapatnekar, "Prediction of leakage power under process uncertainties," in *Proceedings of the ACM Transactions on Design Automation of Electronic Systems*, vol. 12, no. 2, April 2007.

[21] G. Chen, K. Y. Chuah, M. F. Li, D. S. H. Chan, C. H. Ang, J. Z. Cheng, Y. Jin, and D. L. Kwong, "Dynamic NBTI of PMOS transistors and its impact on device lifetime," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 196–200, 2003.

[22] G. Chen, M. F. Li, C. H. Ang, J. Z. Zheng, and D. L. Kwong, "Dynamic NBTI of p-MOS transistors and its impact on MOSFET scaling," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 196–202, 2003.

[23] G. Chen and S. S. Sapatnekar, "Partition-driven standard cell placement," in *Proceedings of the International Symposium on Physical Design*, pp. 75–80, 2003.

[24] Q. Chen, M. Meterelliyoz, and K. Roy, "A CMOS thermal sensor and its applications in temperature adaptive design," in *Proceedings of the IEEE International Symposium on Quality Electronic Design*, 2006.

[25] T. Chen and S. Naffziger, "Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation," *IEEE Transactions on VLSI Systems*, vol. 11, no. 5, pp. 888–899, October 2003.

[26] T.-Y. Chiang, K. Banerjee, and K. C. Saraswat, "Analytical thermal model for multilevel VLSI interconnects incorporating via effect," *IEEE Electron Device Letters*, vol. 23, no. 1, pp. 31–33, January 2002.

[27] R. C. Chu, R. E. Simons, and G. M. Chrysler, "Experimental investigation of an enhanced thermosyphon heat loop for cooling a high performance electronics module," in *Proceedings of the IEEE Semiconductor Thermal Measurement and Management Symposium* (*Semitherm*), pp. 1–9, 1999.

[28] L. O. Chua and P.-M. Lin, *Computed-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*. Englewood Cliffs, NJ: Prentice-Hall, 1975.

[29] P. Cocchini, "Concurrent flip-flop and repeater insertion for high performance integrated circuits," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 268–273, 2002.

[30] J. Cong, J. Fang, and Y. Zhang, "Multilevel approach to full-chip gridless routing," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 234–241, 2001.

[31] J. Cong, A. Jagannathan, G. Reinman, and M. Romesis, "Microarchitecture evaluation with physical planning," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 32–35, 2003.

[32] J. Cong, G. Luo, J. Wei, and Y. Zhang, "Thermal-aware 3D IC placement via transformation," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 780–785, 2007.

[33] J. Cong, J. Wei, and Y. Zhang, "A thermal-driven floorplanning algorithm for 3D ICs," in *Proceedings of the International Symposium on Physical Design*, pp. 306–313, 2004.

[34] J. Cong, M. Xie, and Y. Zhang, "An enhanced multilevel routing system," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 51–58, 2002.

[35] J. Cong and Y. Zhang, "Thermal-driven multilevel routing for 3-D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 121–126, 2005.

[36] J. P. Costa, M. Chou, and L. M. Silveira, "Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 18, no. 5, pp. 597–607, May 1999.

[37] H. Dadgour, S.-C. Lin, and K. Banerjee, "A statistical framework for estimation of full-chip leakage-power distribution under parameter variations," *IEEE Transactions on Electron Devices*, vol. 54, no. 11, pp. 2930–2945, November 2007.

[38] S. Das, A. Chandrakasan, and R. Reif, "Design tools for 3-D integrated circuits," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 53–56, 2003.

[39] A. Dasdan and I. Hom, "Handling inverted temperature dependence in static timing analysis," in *Proceedings of the ACM Transactions on Design Automation of Electronic Systems*, vol. 11, no. 2, pp. 306–324, April 2006.

[40] F. M. d'Heurle, "Electromigration and failure in electronics: An introduction," in *Proceedings of the IEEE*, vol. 59, pp. 1409–1418, October 1971.

[41] P. G. Doyle and J. L. Snell, *Random Walks and Electric Networks*. Washington, DC: Mathematical Association of America, 1984.

[42] M. Ekpanyapong, J. R. Minz, T. Watewai, H.-H. S. Lee, and S. K. Lim, "Profile-guided microarchitectural floorplanning for deep submicron processor design," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 634–639, 2004.

[43] M. Ershov, R. Lindley, S. Saxena, A. Shibkov, S. Minehane, J. Babcock, S. Winters, H. Karbasi, T. Yamashita, P. Clifton, and M. Redford, "Transient effects and characterization methodology of negative bias temperature instability in pMOS transistors," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 606–607, 2003.

[44] T. Fischer, F. Anderson, B. Patella, and S. Naffziger, "A 90 nm variable-frequency clock system for a power-managed itanium®-family processor," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 294–299, 599, 2005.

[45] V. Gerousis, "Design and modeling challenges for 90 nm and 50 nm," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 353–360, 2003.

[46] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 344–353, March 1996.

[47] G. Golub and C. F. V. Loan, *Matrix Computations*. Baltimore, MD: John Hopkins University Press, third ed., 1996.

[48] B. Goplen, *Advanced Placement Techniques for Future VLSI Circuits*. PhD thesis, Minneapolis, MN: University of Minnesota, 2006.

[49] B. Goplen and S. S. Sapatnekar, "Efficient thermal placement of standard cells in 3D ICs using a force directed approach," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 86–89, November 2003.

[50] B. Goplen and S. S. Sapatnekar, "Thermal via placement in 3D ICs," in *Proceedings of the International Symposium on Physical Design*, pp. 167–174, 2005.

[51] B. Goplen and S. S. Sapatnekar, "Placement of thermal vias in 3-D ICs using various thermal objectives," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 26, no. 4, pp. 692–709, April 2006.

[52] B. Goplen and S. S. Sapatnekar, "Placement of 3D ICs with thermal and interlayer via considerations," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 626–631, 2007.

[53] T. Grasser, W. Gos, V. Sverdlov, and B. Kaczer, "The universality of NBTI relaxation and its implications for modeling and characterization," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 268–280, 2007.

[54] K. W. Guarini, A. W. Topol, M. Leong, R. Yu, L. Shi, M. R. Newport, D. J. Frank, D. V. Singh, G. M. Cohen, S. V. Nitta, D. C. Boyd, P. A. O'Neil, S. L. Tempest, H. B. Pogpe, S. Purushotharnan, and W. E. Haensch, "Electrical integrity of state-of-the-art 0.13 μm SOI CMOS devices and circuits transferred for three-dimensional (3D) integrated circuit (IC) fabrication," in *IEEE International Electronic Devices Meeting*, pp. 943–945, 2002.

[55] H. Gunther, F. Binns, D. M. Carmean, and J. C. Hall, "Managing the impact of increasing microprocessor power consumption," *Intel Technology Journal*, vol. 5, no. 1, February 2001.

[56] R. T. Hadsell and P. H. Madden, "Improved global routing through congestion estimation," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 28–34, 2003.

[57] Y. Han, I. Koren, and C. A. Moritz, "Temperature aware floorplanning," in *Second Workshop on Temperature-Aware Computing Systems*, 2005.

[58] S. Hassoun, C. J. Alpert, and M. Thiagarajan, "Optimal buffered routing path constructions for single and multiple clock domain systems," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 247–253, 2002.

[59] M. Healy, M. Vittes, M. Ekpanyapong, C. Ballapuram, S. K. Lim, H.-H. S. Lee, and G. H. Loh, "Microarchitectural floorplanning under performance and thermal tradeoff," in *Proceedings of the Design, Automation and Test in Europe*, pp. 1–6, 2006.

[60] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron, and M. R. Stan, "HotSpot: A compact thermal modeling methodology for early-stage VLSI design," *IEEE Transactions on VLSI Systems*, vol. 14, no. 5, pp. 501–513, May 2006.

[61] W. Huang, K. Sankaranarayanan, R. J. Ribando, M. R. Stan, and K. Skadron, "An improved block-based thermal model in HotSpot 4.0 with granularity considerations," Tech. Rep. CS-2007-07, Department of Computer Science, University of Virginia, Charlottesville, VA, 2007.

[62] W. Huang, K. Sankaranarayanan, R. J. Ribando, M. R. Stan, and K. Skadron, "An improved block-based thermal model in HotSpot 4.0 with granularity considerations," in *Proceedings of the Workshop on Duplicating, Deconstructing, and Debunking*, 2007.

[63] W. Huang, M. R. Stan, and K. Skadron, "Parameterized physical compact thermal modeling," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 4, pp. 615–622, December 2005.

[64] W. Huang, M. R. Stan, K. Skadron, K. Sankaranarayanan, S. Ghosh, and S. Velusamy, "Compact thermal modeling for temperature-aware design," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 878–883, 2004.

[65] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modeling," *Journal of Microelectronics Reliability*, vol. 46, pp. 1–23, January 2006.

[66] V. Huard, C. R. Parthasarathy, C. Guerin, and M. Denais, "Physical modeling of negative bias temperature instabilities for predictive exploration," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 733–734, 2006.

[67] A. E. Islam, H. Kufluoglu, D. Varghese, and M. A. Alam, "Critical analysis of short-term negative bias temperature instability measurements: Explaining the effect of time-zero delay for on-the-fly measurements," *Applied Physics Letters*, vol. 90, February 2007.

[68] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A.Alam, "Recent issues in negative bias temperature instability: Initial degradation, field dependence of interface trap generation, hole trapping effects, and relaxation," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2143–2154, September 2007.

[69] A. Jagannathan et al., "Microarchitecture evaluation with floorplanning and interconnect pipelining," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 8–15, January 2005.

[70] M. Janicki, G. De Mey, and A. Napieralski, "Transient thermal analysis of multilayered structures using Green's functions," *Microelectronics and Reliability*, vol. 42, pp. 1059–1064, 2002.

[71] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of NMOS devices," *Journal of Applied Physics*, vol. 48, pp. 2004–2014, 1977.

[72] Y. Joshi, "Emerging thermal challenges in electronics driven by performance, reliability and energy efficiency," in *8th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2002.

[73] B. Kaczer, V. Arkhipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin, "Disorder-controlled kinetics model for NBTI and its experimental verification," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 381–387, 2005.

[74] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design impact of positive temperature dependence on drain current in Sub-1-V CMOS VLSIs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1559–1564, October 2001.

[75] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, "NBTI impact on transistor and circuit: Models, mechanisms and scaling effects," in *IEEE International Electronic Devices Meeting*, pp. 14.5.1–14.5.4, 2003.

[76] S. H. Kulkarni, D. Sylvester, and D. Blaauw, "A statistical framework for post-silicon tuning through body bias clustering," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 39–46, 2006.

[77] S. V. Kumar, C. H. Kim, , and S. S. Sapatnekar, "An analytical model for negative bias temperature instability (NBTI)," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 493–496, 2006.

[78] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Mathematically-assisted adaptive body bias (ABB) for temperature compensation in gigascale LSI systems," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 559–564, 2006.

[79] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 370–375, 2007.

[80] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Body bias voltage computations for process and temperature compensation," *IEEE Transactions on VLSI Systems*, vol. 16, no. 3, pp. 249–262, March 2008.

[81] T. Kuroda, T. Fujita, S. Mita, T. Nagamatu, S. Yoshioka, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu, and T. Sakurai, "A 0.9 V 150 MHz 10 mW 2-D discrete cosine transform core processor with variable-threshold-voltage scheme," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 166–167, 1996.

[82] B. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," *IEEE International Electronic Devices Meeting*, pp. 133–136, 1999.

[83] D. Lee, D. Blaauw, and D. Sylvester, "Static leakage reduction through simultaneous V_t/T_{ox} and state assignment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 7, pp. 1014–1029, July 2005.

[84] P. Li, L. T. Pileggi, M. Asheghi, and R. Chandra, "Efficient full-chip thermal modeling and analysis," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 319–326, November 2004.

[85] P. Li, L. T. Pileggi, M. Asheghi, and R. Chandra, "IC thermal simulation and modeling via efficient multigrid-based approaches," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 25, no. 9, pp. 1763–1776, September 2006.

[86] J.-M. Lin and Y.-W. Chang, "TCG: A transitive closure graph based representation for non-slicing floorplans," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 764–769, 2001.

[87] D. L. Logan, *A First Course in the Finite Element Method*. Pacific Grove, CA: Brooks/Cole Publishing Company, third ed., 2002.

[88] C. Long, L. J. Simonson, W. Liao, and L. He, "Floorplanning optimization with trajectory piecewise-linear model for pipelined interconnects," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 640–645, 2004.

[89] R. Mahajan, C.-P. Chiu, and G. Chrysler, "Cooling a microprocessor chip," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1476–1486, August 2006.

[90] S. Mahapatra, K. Ahmed, S. Varghese, A. E. Islam, G. Gupta, L. Madhav, D. Saha, and M. A. Alam, "On the physical mechanism of NBTI in silicon oxynitride p-MOSFETs: Can differences in insulator processing conditions resolve the interface trap generation versus hole trapping controversy?," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 1–9, 2007.

[91] S. M. Martin, K. Flautner, T. Mudge, and D. Blaauw, "Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 721–725, 2002.

[92] J. G. Massey, "NBTI: What we know and what we need to know — A tutorial addressing the current understanding and challenges for the future," in *Proceedings of the IEEE International Integrated Reliability Workshop Final Report*, pp. 199–211, 2004.

[93] R. McGowen, C. A. Poirier, C. Bostak, J. Ignowski, M. Millican, W. H. Parks, and S. Naffziger, "Power and temperature control on a 90-nm Itanium family processor," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 229–237, January 2006.

[94] M. Miyazaki, G. Ono, and T. Kawahara, "Optimum threshold-voltage tuning for low-power high-performance microprocessor," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 17–20, 2005.

[95] D. C. Montgomery, *Design and Analysis of Experiments*. New York, NY: John Wiley, 1991.

[96] S. Mukhopadhyay, A. Raychowdury, K. Roy, and C. Kim, "Accurate estimation of total leakage in nanometer-scale bulk CMOS circuits based on device geometry and doping profile," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 3, pp. 363–381, March 2005.

[97] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V power supply high-speed digital circuit technology with multithreshold voltage CMOS," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 847–854, August 1995.

[98] S. Narendra, A. Keshavarzi, B. A. Bloechel, S. Borkar, and V. De, "Forward body bias for microprocessors in 130-nm technology generation and beyond," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 5, pp. 696–701, May 2003.

[99] V. Nookala, Y. Chen, D. J. Lilja, and S. S. Sapatnekar, "Microarchitecture-aware floorplanning using a statistical design of experiments approach," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 579–584, 2005.

[100] V. Nookala, D. J. Lilja, and S. S. Sapatnekar, "Temperature-aware floorplanning of microarchitecture blocks with IPC-power dependence modeling and transient analysis," in *Proceedings of the ACM International Symposium on Low Power Electronics and Design*, pp. 298–303, 2006.

[101] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si-SiO2 interface," *Journal of Applied Physics*, vol. 51, pp. 4128–4230, February 1995.

[102] G. Ono, M. Miyazaki, H. Tanaka, N. Ohkubo, and T. Kawahara, "Temperature referenced supply voltage and forward-body-bias control (TSFC) architecture for minimum power consumption," in *Proceedings of the European Solid State Circuits Conference*, pp. 391–394, 2004.

[103] A. V. Oppenheim, R. W. Schafer, and J. R. Buck, *Discrete-Time Signal Processing*. Upper Saddle River, NJ: Prentice Hall, 1999.

[104] M. N. Özişik, *Heat Transfer: A Basic Approach*. New York, NY: McGraw-Hill, 1985.

[105] C. R. Parthasarathy, M. Denais, V. Huard, G. Ribes, E. Vincent, and A. Bravaix, "New insights into recovery characteristics post NBTI stress," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 471–477, 2006.

[106] B. C. Paul, K. Kang, H. Kufluoglu, M. A. Alam, and K. Roy, "Impact of NBTI on the temporal performance degradation of digital circuits," *IEEE Electron Device Letters*, vol. 26, pp. 560–562, August 2003.

[107] B. C. Paul, K. Kang, H. Kufluoglu, M. A. Alam, and K. Roy, "Temporal performance degradation under NBTI: Estimation and design for improved reliability of nanoscale circuits," in *Proceedings of the Design, Automation and Test in Europe*, pp. 1–6, 2006.

[108] C. Piorier, R. McGowen, C. Bostak, and S. Naffziger, "Power and temperature control on an Itanium®-family processor," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 304–305, 2005.

[109] E. Pop, R. W. Dutton, and K. E. Goodson, "Analytic band Monte Carlo model for electron transport in Si including acoustic and optical phonon disperson," *Journal of Applied Physics*, vol. 96, no. 9, pp. 4998–5005, 2004.

[110] E. Pop, S. Sinha, and K. E. Goodson, "Heat generation and transport in nanometer-scale transistors," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1587–1601, August 2006.

[111] R. Prasher, "Thermal interface materials: Historical perspective, status, and future directions," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1571–1586, August 2006.

[112] H. Qian, *Stochastic and Hybrid Linear Equation Solvers and their Applications in VLSI Design Automation*. PhD thesis, Minneapolis, MN: University of Minnesota, 2006.

[113] H. Qian, S. R. Nassif, and S. S. Sapatnekar, "Random walks in a supply network," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 93–98, 2003.

[114] H. Qian, S. R. Nassif, and S. S. Sapatnekar, "Power grid analysis using random walks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 8, pp. 1204–1224, August 2005.

[115] H. Qian and S. S. Sapatnekar, "Hierarchical random-walk algorithms for power grid analysis," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 499–504, 2004.

[116] H. Qian and S. S. Sapatnekar, "A hybrid linear equation solver and its application in quadratic placement," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 905–909, November 2005.

[117] H. Qian and S. S. Sapatnekar, "Stochastic preconditioning for iterative linear equation solvers," *SIAM Journal on Scientific Computing*, vol. 30, no. 3, pp. 1178–1204, March 2008.

[118] V. Reddy, A. T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T. Rost, and S. Krishnan, "Impact of negative bias temperature instability on digital circuit reliability," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 248–254, April 2002.

[119] R. Reif, A. Fan, K.-N. Chen, and S. Das, "Fabrication technologies for three-dimensional integrated circuits," in *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 33–37, 2002.

[120] H. Reisenger, O. Blank, W. Heinrigs, W. Gustin, and C. Schlunder, "A comparison of very fast to very slow components in degradation and recovery due to NBTI and bulk hole trapping to existing physical models," *IEEE Transactions on Devices and Materials Reliability*, vol. 7, pp. 119–129, March 2007.

[121] H. Reisenger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI degradation and recovery behavior based on ultra fast Vt measurements," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 448–453, 2006.

[122] P. Rodgers, V. Eveloy, and M. G. Pecht, "Extending the limits of air-cooling in microelectronic equipment," in *International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems* (*EumSimE*), pp. 695–702, 2005.

[123] J. Rowlette, E. Pop, S. Sinha, M. Panzer, and K. Goodson, "Thermal simulation techniques for nanoscale transistors," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 225–228, November 2005.

[124] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-micrometer CMOS circuits," in *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, February 2003.

[125] H. Sanchez, B. Kuttanna, T. Olson, M. Alexander, G. Gerosa, R. Philip, and J. Alvarez, "Thermal management system for high performance PowerPC$^{\text{TM}}$ microprocessors," in *Proceedings of the IEEE COMPCON*, pp. 325–330, 1997.

[126] K. Sankaranarayanan, S. Velusamy, M. Stan, and K. Skadron, "A case for thermal-aware floorplanning at the microarchitectural level," *The Journal of Instruction-Level Parallelism*, vol. 8, September 2005.

[127] S. S. Sapatnekar, *Timing*. Boston, MA: Springer, 2004.

[128] S. S. Sapatnekar and H. Su, "Analysis and optimization of power grids," *IEEE Design and Test*, vol. 20, no. 3, pp. 7–15, May–June 2002.

[129] P. Saxena, N. Menezes, P. Cocchini, and D. A. Kirkpatrick, "Repeater scaling and its impact on CAD," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 23, no. 4, pp. 451–463, April 2004.

[130] D. K. Schroder, "Negative bias temperature instability: Physics, materials, process, and circuit issues," available at http://www.ewh.ieee.org/r5/denver/sscs/Presentations/2005.08.Schroder.p%df, 2005.

[131] A. Shakouri, "Nanoscale thermal transfer and microrefrigerators on a chip," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1613–1638, August 2006.

[132] J. Sharp, J. Bierschenk, and H. B. Lyon, Jr., "Overview of solid-state thermal microrefrigerators and possible applications to on-chip thermal management," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1602–1612, August 2006.

[133] C. Shen, M. F. Li, C. E. Foo, T. Yang, D. M. Huang, A. Yap, G. S.Samudra, and Y.-C. Yeo, "Characterization and physical origin of fast V_{th} transient in

NBTI of pMOSFETs with SiON dielectric," in *IEEE International Electronic Devices Meeting*, pp. 333–336, 2006.

[134] S. Sinha, E. Pop, R. W. Dutton, and K. E. Goodson, "Non-equilibrium phonon distribution in sub 100 nm silicon transistors," *Transactions of the ASME*, vol. 28, pp. 638–647, July 2006.

[135] K. Skadron, T. Abdelzaher, and M. Stan, "Control-theoretic techniques and thermal-RC modeling for accurate and localized dynamic thermal management," in *Proceedings of the Eighth International Symposium on High-Performance Computer Architecture*, pp. 17–28, 2002.

[136] K. Skadron, K. Sankaranarayanan, S. Velusamy, D. Tarjan, M. Stan, and W. Huang, "Temperature-aware microarchitecture: Modeling and implementation," *ACM Transactions on Architecture and Code Optimization*, vol. 1, no. 1, pp. 94–125, March 2004.

[137] K. Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayan, and D. Tarjan, "Temperature-aware microarchitecture," in *Proceedings of the ACM International Symposium on Computer Architecture*, pp. 2–13, 2003.

[138] J. H. Stathis, "Reliability limites for the gate insulator in CMOS technology," *IBM Journal of Research and Development*, vol. 46, pp. 265–286, March/May 2002.

[139] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Journal of Microelectronics Reliability*, vol. 46, pp. 270–286, February–April 2006.

[140] L. M. Ting, J. S. May, W. R. Hunter, and J. W. McPherson, "AC electromigration characterization and modeling of multilayered interconnects," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 311–316, 1993.

[141] C. H. Tsai and S. M. Kang, "Cell-level placement for improving substrate thermal distribution," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 19, no. 2, pp. 253–266, Feburary 2000.

[142] J.-L. Tsai, C. C.-P. Chen, G. Chen, B. Goplen, H. Qian, Y. Zhan, S.-M. Kang, M. D. F. Wong, and S. S. Sapatnekar, "Temperature-aware placement for SOCs," in *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1502–1518, August 2006.

[143] J. Tschanz, S. Narendra, A. Keshavarazi, and V. De, "Adaptive circuit techniques to minimize variation impacts on microprocessor performance and power," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 9–12, 2005.

[144] J. W. Tschanz, J. Kao, S. G. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, November 2002.

[145] J. W. Tschanz, N. S. Kim, S. Dighe, J. Howard, G. Ruhl, S. Vangal, S. Narendra, Y. Hoskote, H. Wilson, C. Lam, M. Shuman, C. Tokunaga, D. Somasekhar, S. Tang, D. Flnan, T. Karnik, N. Borkar, N. Kurd, and V. De, "Adaptive frequency and biasing techniques for tolerance to dynamic

temperature-voltage variations and aging," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 292–294, 2007.

[146] J. W. Tschanz, S. G. Narendra, R. Nair, and V. De, "Effectiveness of adaptive supply voltage and body bias for reducing impact of parameter variations in low power and high performance microprocessors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 5, pp. 826–829, May 2003.

[147] J. W. Tschanz, S. G. Narendra, Y. Ye, B. A. Bloechel, S. Borkar, and V. De, "Dynamic sleep transistor and body bias for active leakage power control of microprocessors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 11, pp. 1838–1845, November 2003.

[148] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 1047–1052, 2006.

[149] N. Viswanathan and C. C.-N. Chu, "FastPlace: Efficient analytical placement using cell shifting, iterative local refinement and a hybrid net model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 5, pp. 722–733, May 2005.

[150] B. Wang and P. Mazumder, "Fast thermal analysis for vlsi circuits via semi analytical Greens functions in multi-layer 3-D integrated circuits," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2004.

[151] B. Wang and P. Mazumder, "A logarithmic complexity algorithm for full chip thermal analysis using multi-layer Greens function," in *Proceedings of the Design, Automation and Test in Europe*, 2006.

[152] B. Wang and P. Mazumder, "Accelerated chip-level thermal analysis using multilayer green's function," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 26, no. 2, pp. 325–344, February 2007.

[153] T.-Y. Wang and C. C.-P. Chen, "3-D Thermal-ADI: A linear-time chip level transient thermal simulator," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 21, no. 12, pp. 1434–1445, December 2002.

[154] C. H. Wann, H. Chenming, K. Noda, D. Sinitsky, F. Assaderaghi, and J. Bokor, "Channel doping engineering of MOSFET with adaptable threshold voltage using body effect for low voltage and low power applications," in *Proceedings of the IEEE International Symposium of VLSI Technology*, pp. 159–163, 1995.

[155] J. Westra, C. Bartels, and P. Groeneveld, "Probabilistic congestion prediction," in *Proceedings of the International Symposium on Physical Design*, pp. 204–209, 2004.

[156] E. Wong and S. K. Lim, "3D floorplanning with thermal vias," in *Proceedings of the Design, Automation and Test in Europe*, pp. 878–883, 2006.

[157] E. Wu, E. Nowak, A. Vayshenker, J. McKenna, D. Harmon, and R. Vollertsen, "New global insight in ultra-thin oxide reliability using accurate experimental methodology and comprehensive database," *IEEE Transactions on Devices and Materials Reliability*, vol. 1, pp. 69–80, 2001.

[158] E. Y. Wu, E. J. Nowak, A. Vayshenker, W. L. Lai, and D. L. Harmon, "CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics," *IBM Journal of Research and Development*, vol. 46, pp. 287–298, March/May 2002.

[159] Y. W. Wu, C.-L. Yang, P.-H. Yuh, and Y.-W. Chang, "Joint exploration of architectural and physical design spaces with thermal consideration," in *Proceedings of the ACM International Symposium on Low Power Electronics and Design*, pp. 123–126, 2005.

[160] R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe, "SMARTS: Accelerating microarchitecture simulation via rigorous statistical sampling," in *Proceedings of the ACM International Symposium on Computer Architecture*, pp. 84–97, 2003.

[161] S. Yajuan, W. Zuodong, and W. Shaojun, "Energy-aware Supply and Body Biasing Voltage Scheduling Algorithm," in *Proceedings of the International Conference on Solid State and Integrated Circuits Technology*, pp. 1956–1959, 2004.

[162] L. Yan, J. Luo, and N. K. Jha, "Combined dynamic voltage scaling and adaptive body biasing for heterogeneous distributed real-time embedded systems," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 30–37, 2003.

[163] L. Yan, J. Luo, and N. K. Jha, "Joint dynamic voltage scaling and adaptive body biasing for heterogeneous distributed real-time embedded systems," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 24, no. 7, pp. 1030–1041, July 2005.

[164] Y. Yang, C. Zhu, Z. Gu, L. Shang, and R. P. Dick, "Adaptive multi-domain thermal modeling and analysis for integrated circuit synthesis and design," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 575–582, 2006.

[165] R. D. Yates and D. J. Goodman, *Probability and Stochastic Processes: A Friendly Introduction for Electrical and Computer Engineers*. New York, NY: John Wiley and Sons, 1999.

[166] S. Zafar, B. H. Lee, J. Stathis, A. Callegari, and T. Ning, "A model for negative bias temperature instability (NBTI) in oxide and high k pFETs," in *Proceedings of the IEEE Symposium on VLSI Technology*, pp. 208–209, 2004.

[167] Y. Zhan and S. S. Sapatnekar, "High efficiency Green function-based thermal simulation algorithms," *IEEE Transactions on Computer-Aided Design of Integrated*, vol. 26, no. 9, pp. 1661–1675, September 2007.

[168] S. Zhang and K. S. Chatha, "Approximation algorithm for the temperature-aware scheduling problem," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 281–288, 2007.

[169] T. Zhang, Y. Zhan, and S. S. Sapatnekar, "Temperature-aware routing in 3D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 309–314, 2006.

[170] P. Zhou, Y. Ma, Z. Li, R. P. Dick, L. Shang, H. Zhou, X. Hong, and Q. Zhou, "3D-STAF: Scalable temperature and leakage aware floorplanning for three-dimensional integrated circuits," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 590–597, 2007.

[171] B. Zhu, J. S. Suehle, Y. Chen, and J. B. Bernstein, "Negative bias temperature instability of deep sub-micron p-MOSFETs under pulsed bias stress," in *Proceedings of the IEEE International Integrated Reliability Workshop Final Report*, pp. 125–129, 2002.