# Three-dimensional Integrated Circuits: Design, EDA, and Architecture

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## Abstract

The emerging three-dimensional (3D) integration technology is one of the promising solutions to overcome the barriers in interconnection scaling, thereby offering an opportunity to continue performance improvements using CMOS technology. As the fabrication of 3D integrated circuits has become viable, developing CAD tools and architectural techniques are imperative for the successful adoption of 3D integration technology. In this article, we first give a brief introduction on the 3D integration technology, and then review the EDA challenges and solutions that can enable the adoption of 3D ICs, and finally present design and architectural techniques on the application of 3D ICs, including a survey of various approaches to design future 3D ICs, leveraging the benefits of fast latency, higher bandwidth, and heterogeneous integration capability that are offered by 3D technology.

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# 1

# Introduction

With continued technology scaling, interconnection has emerged as the dominant source of circuit delay and power consumption. The reduction of interconnect delays and power consumption are of paramount importance for deep-sub-micron designs. Three-dimensional integrated circuits (3D ICs) [1] are attractive options for overcoming the barriers in interconnection scaling, thereby offering an opportunity to continue performance improvements using CMOS technology.

3D integration technologies offer many benefits for future microprocessor designs. Such benefits include: (1) *The reduction in interconnection wire length*, which results in improved performance and reduced power consumption; (2) *Improved memory bandwidth*, by stacking memory on microprocessor cores with TSV connections between the memory layer and the core layer; (3) *The support for realization of heterogeneous integration*, which could result in novel architecture designs. (4) *Smaller form factor*, which results in higher packing density and smaller footprint due to the addition of a third dimension to the conventional two dimensional layout, and potentially results in a lower cost design.

This monograph first presents the background on 3D integration technologies, and shows the major benefits offered by 3D integration.

As a key part, EDA design tools and methodologies for 3D ICs are reviewed. The designs of 3D FPGAs and micro-architectures are then discussed, which leverage the benefits of fast latency, higher bandwidth, and heterogeneous integration capability that are offered by 3D technologies. The cost of 3D integration is also analyzed in the last section.

# References

[1] W. R. Davis, J. Wilson, S. Mick, et al. Demystifying 3D ICs: the pros and cons of going vertical. *IEEE Design and Test of Computers*, 22(6):498–510, 2005.

[2] Y. Xie, G Loh, B Black, and K. Bernstein. Design space exploration for 3D architectures. *ACM Journal of Emerging Technologies in Compuing Systems*, 2006.

[3] Yuan Xie, Jason Cong, and Sachin Sapatnekar. *Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures*. Springer, 2009.

[4] Yuan Xie. Processor architecture design using 3D integration technology. In *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, pages 446–451, jan. 2010.

[5] P. Garrou. *Handbook of 3D Integration: Technology and Applications using 3D Integrated Circuits*, chapter Introduction to 3D Integration. Wiley-CVH, 2008.

[6] J.W. Joyner, P. Zarkesh-Ha, and J.D. Meindl. A stochastic global net-length distribution for a three-dimensional system-on-a-chip (3D-SoC). In *Proc. 14th Annual IEEE International ASIC/SOC Conference*, September 2001.

[7] Yuh-fang Tsai, Feng Wang, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. Design space exploration for three-dimensional cache. *IEEE Transactions on Very Large Scale Integration Systems*, 2008.

[8] Balaji Vaidyanathan, Wei-Lun Hung, Feng Wang, Yuan Xie, Vijaykrishnan Narayanan, and Mary Jane Irwin. Architecting microprocessor components in 3D design space. In *Intl. Conf. on VLSI Design*, pages 103–108, 2007.

[9] Kiran Puttaswamy and Gabriel H. Loh. Scalability of 3D-integrated arithmetic units in high-performance microprocessors. In *Design Automation Conference*, pages 622–625, 2007.

[10] Jin Ouyang, Guangyu Sun, Yibo Chen, Lian Duan, Tao Zhang, Yuan Xie, and Mary Irwin. Arithmetic unit design using 180nm TSV-based 3D stacking technology. In *IEEE International 3D System Integration Conference*, 2009.

[11] R Egawa, J Tada, H Kobayashi, and G Goto. Evaluation of fine grain 3D integrated arithmetic units. In *IEEE International 3D System Integration Conference*, 2009.

[12] Bryan Black, Murali Annavaram, Ned Brekelbaum, John DeVale, Lei Jiang, Gabriel H. Loh, Don McCaule, Pat Morrow, Donald W. Nelson, Daniel Pantuso, Paul Reed, Jeff Rupley, Sadasivan Shankar, John Shen, and Clair Webb. Die stacking (3D) microarchitecture. In *MICRO 39: Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture*, pages 469–479, Washington, DC, USA, 2006. IEEE Computer Society.

[13] Gabriel H. Loh. 3D-stacked memory architectures for multi-core processors. In *ISCA '08: Proceedings of the 35th Annual International Symposium on Computer Architecture*, pages 453–464, Washington, DC, USA, 2008. IEEE Computer Society.

[14] P. Jacob et al. Mitigating memory wall effects in high clock rate and multicore cmos 3D ICs: Processor memory stacks. *Proceedings of IEEE*, 96(10), 2008.

[15] Gabriel Loh, Yuan Xie, and Bryan Black. Processor design in three-dimensional die-stacking technologies. *IEEE Micro*, 27(3):31–48, 2007.

[16] Taeho Kgil, Shaun D'Souza, Ali Saidi, Nathan Binkert, Ronald Dreslinski, Trevor Mudge, Steven Reinhardt, and Krisztian Flautner. PicoServer: using 3D stacking technology to enable a compact energy efficient chip multiprocessor. In *ASPLOS*, pages 117–128, 2006.

[17] S. Vangal et al. An 80-tile Sub-100-W TeraFLOPS processor in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, 43(1):29–41, 2008.

[18] Gabriel H. Loh. Extending the effectiveness of 3D-stacked DRAM caches with an adaptive multi-queue policy. In *MICRO 42: Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture*, pages 201–212, New York, NY, USA, 2009. ACM.

[19] Feihui Li, Chrysostomos Nicopoulos, Thomas Richardson, Yuan Xie, Vijaykrishnan Narayanan, and Mahmut Kandemir. Design and management of 3D chip multiprocessors using network-in-memory. In *ISCA '06: Proceedings of the 33rd annual international symposium on Computer Architecture*, pages 130–141, Washington, DC, USA, 2006. IEEE Computer Society.

[20] Xiangyu Dong, Xiaxiao Wu, Guangyu Sun, et al. Circuit and microarchitecture evaluation of 3D stacking Magnetic RAM (MRAM) as a universal memory replacement. In *Proceedings of the Design Automation Conference*, pages 554–559, 2008.

[21] Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, and Yuan Xie. Hybrid cache architecture. In *International Symposium on Computer Architecture (ISCA)*, 2009.

[22] Guangyu Sun, Xiangyu Dong, Yuan Xie, Jian Li, and Yiran Chen. A novel 3D stacked MRAM cache architecture for CMPs. In *International Symposium on High Performance Computer Architecture*, 2009.

[23] Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P. Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G. Beausoleil, and Jung Ho Ahn. Corona: System implications of emerging nanophotonic technology. In *ISCA '08: Proceedings of the 35th Annual International Symposium on Computer Architecture*, pages 153–164, Washington, DC, USA, 2008. IEEE Computer Society.

[24] Xiangyu Dong and Yuan Xie. Cost analysis and system-level design exploration for 3D ICs. In *Asia and South Pacific Design Automation Conference*, 2009.

[25] S.S. Sapatnekar. Addressing Thermal and Power Delivery Bottlenecks in 3D Circuits. In *Proceedings of the Asia and South Pacific Design Automation Conference, 2009.*, pages 423–428, 2009.

[26] Peng Li, L. T. Pileggi, M. Asheghi, and R. Chandra. IC thermal simulation and modeling via efficient multigrid-based approaches. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25:1763–1776, 2006.

[27] Brent Goplen and Sachin Sapatnekar. Efficient Thermal Placement of Standard Cells in 3D ICs using a Force Directed Approach. *Proceedings of ICCAD*, 2003.

[28] W. Huang, S. Ghosh, and et al. Hotspot: a compact thermal modeling methodology for early-stage VLSI design. *TVLSI*, 14(5):501–513, 2006.

[29] G. M. Link and N. Vijaykrishnan. Thermal trends in emerging technologies. pages 625–632, 2006.

[30] J. Cong and Yan Zhang. Thermal-driven multilevel routing for 3D ICs. In *Proc. Asia and South Pacific Design Automation Conf the ASP-DAC 2005*, volume 1, pages 121–126, 2005.

[31] Y. Yang, Z. Gu, C. Zhu, R. P. Dick, and L. Shang. ISAC: Integrated space-and-time-adaptive chip-package thermal analysis. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 26(1):86–99, 2007.

[32] W. Hung, G. Link, Y. Xie, V. Narayanan, and M.J.Irwin. Interconnect and thermal-aware floorplanning for 3D microprocessors. In *Proceedings of the International Symposium of Quality Electronic Devices*, 2006.

[33] J. Cong, J. Wei, and Y. Zhang. A thermal-driven floorplanning algorithm for 3d ics. In *Proceedings of the ICCAD*, 2004.

[34] C. Chu and D. Wong. A matrix synthesis approach to thermal placement. In *Proceedings of the ISPD*, 1997.

[35] C. Tsai and S. Kang. Cell-level placement for improving substrate thermal distributio. In *IEEE Trans. on Computer-Aided Design of Integrated Circuits and System*, 2000.

[36] P. Shiu and S. K. Lim. Multi-layer floorplanning for reliable system-on-package. In *Proceedings of ISCAS*, 2004.

[37] Y. Chang, Y. Chang, G.-M. Wu, and S.-W. Wu. B*-trees: a new representation for non-slicing floorplans . *Proceedings of the Annual ACM/IEEE Design Automation Conference*, 2000.

[38] Karthik Balakrishnan, Vidit Nanda, Siddharth Easwar, and Sung Kyu Lim. Wire congestion and thermal aware 3D global placement. In *Proc. of Asia South Pacific Design Automation Conference (ASPDAC)*, pages 1131–1134, 2005.

[39] Jason Cong, Guojie Luo, Jie Wei, and Yan Zhang. Thermal-aware 3D IC placement via transformation. In *Proc. Asia and South Pacific Design Automation Conf. ASP-DAC '07*, pages 780–785, 2007.

[40] J. Cong and Guojie Luo. A multilevel analytical placement for 3D ICs. In *Proc. Asia and South Pacific Design Automation Conf. ASP-DAC 2009*, pages 361–366, 2009.

[41] J. Cong and Y. Zhang. Thermal-Driven Multilevel Routing for 3-D ICs. In *Proc. the Asia South Pacific Design Automation Conference*, January 2005.

[42] J. Cong and Zhang Yan. Thermal via planning for 3-D ICs. In *IEEE/ACM International Conference on Computer-Aided Design.*, pages 745–752, 2005.

[43] Xin Zhao, D. L. Lewis, H.-H. S. Lee, and Sung Kyu Lim. Pre-bond testable low-power clock tree design for 3D stacked ics. In *Proc. IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, pages 184–190, 2009.

[44] Tak-Yung Kim and Taewhan Kim. Clock tree synthesis with pre-bond testability for 3D stacked IC designs. In *Proc. 47th ACM/IEEE Design Automation Conf. (DAC)*, pages 723–728, 2010.

[45] J. R. Minz, Eric Wong, M. Pathak, and Sung Kyu Lim. Placement and routing for 3-D system-on-package designs. *IEEE Trans. Compon. Packag. Technol.*, 29(3):644–657, 2006.

[46] Eric Wong, J. Minz, and Sung Kyu Lim. Multi-objective module placement for 3-D system-on-package. *IEEE Trans. VLSI Syst.*, 14(5):553–557, 2006.

[47] E. Wong, J. Minz, and Sung Kyu Lim. Effective thermal via and decoupling capacitor insertion for 3D system-on-package. In *Proc. 56th Electronic Components and Technology Conf*, 2006.

[48] Hao Yu, J. Ho, and Lei He. Simultaneous power and thermal integrity driven via stapling in 3D ICs. In *Proc. IEEE/ACM Int. Conf. Computer-Aided Design ICCAD '06*, pages 802–808, 2006.

[49] Chen-Wei Liu and Yao-Wen Chang. Power/ground network and floorplan cosynthesis for fast design convergence. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 26(4):693–704, 2007.

[50] P. Falkenstern, Yuan Xie, Yao-Wen Chang, and Yu Wang. Three-dimensional integrated circuits (3D IC) floorplan and power/ground network co-synthesis. In *Proc. 15th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pages 169–174, 2010.

[51] D. L. Lewis and H.-H. S. Lee. A scanisland based design enabling prebond testability in die-stacked microprocessors. In *Proc. IEEE Int. Test Conf. ITC 2007*, pages 1–8, 2007.

[52] D. L. Lewis and H.-H. S. Lee. Testing circuit-partitioned 3D IC designs. In *Proc. IEEE Computer Society Annual Symp. VLSI ISVLSI '09*, pages 139–144, 2009.

[53] Po-Yuan Chen, Cheng-Wen Wu, and Ding-Ming Kwai. On-chip TSV testing for 3D IC before bonding using sense amplification. In *Proc. of Asian Test Symp (ATS)*, pages 450–455, 2009.

[54] H.-H. S. Lee and K. Chakrabarty. Test challenges for 3D integrated circuits. *IEEE Design & Test of Computers*, 26(5):26–35, 2009.

[55] X. Wu, P. Falkenstern, K. Chakrabarty, and Y. Xie. Scan-chain design and optimization for 3D ICs. *ACM Journal of Emerging Technologies for Computer Systems*, 2009.

[56] X. Wu, Y. Chen, K. Chakrabarty, and Y. Xie. Test-access mechanism optimization for core-based three-dimensional SOCs. *Proc. International Conference on Computer Design*, 2008.

[57] Li Jiang, Lin Huang, and Qiang Xu. Test architecture design and optimization for three-dimensional SoCs. In *Proc. DATE '09. Design, Automation & Test in Europe Conf. & Exhibition*, pages 220–225, 2009.

[58] K. Zhang et al. A SRAM Design on 65nm CMOS technology with Integrated Leakage Reduction Scheme. *IEEE Symp. On VLSI Circuits Digest of Technical Papers*, 2004.

[59] Yuhfang Tsai, Yuan Xie, Vijaykrishnan Narayanan, and Mary Jane Irwin. Three-dimensional cache design exploration using 3DCacti. *Proceedings of the IEEE International Conference on Computer Design (ICCD 2005)*, pages 519–524, 2005.

[60] P. Shivakumar et al. Cacti 3.0: An Integrated Cache Timing, Power, and Area Model. *Western Research Lab Research Report*, 2001.

[61] Yibo Chen, Jishen Zhao, and Yuan Xie. 3D-nonFAR: three-dimensional non-volatile FPGA architecture using phase change memory. In *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design*, ISLPED '10, 2010.

[62] C. Ababei, H. Mogal, and K. Bazargan. Three-dimensional place and route for FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25(6):1132–1140, 2006.

[63] M. J. Alexander, J. P. Cohoon, J. L. Colflesh, J. Karro, and G. Robins. Three-dimensional field-programmable gate arrays. In *Proc. Eighth Annual IEEE Int. ASIC Conf. and Exhibit*, pages 253–256, 1995.

[64] S. M. S. A. Chiricescu and M. M. Vai. A three-dimensional FPGA with an integrated memory for in-application reconfiguration data. In *Proc. IEEE Int. Symp. Circuits and Systems ISCAS '98*, volume 2, pages 232–235, 1998.

[65] A. Rahman, S. Das, and et al. Wiring requirement and three-dimensional integration technology for field programmable gate arrays. *TVLSI*, 11(1):44–54, 2003.

[66] M. Lin, A. El Gamal, and et al. Performance benefits of monolithically stacked 3-D FPGA. *TCAD*, 26(2):216–229, 2007.

[67] A. Gayasen, V. Narayanan, M. Kandemir, and A. Rahman. Designing a 3-D FPGA: Switch box architecture and thermal issues. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 16(7):882–893, 2008.

[68] M. Leeser, W. M. Meleis, M. M. Vai, S. Chiricescu, Weidong Xu, and P. M. Zavracky. Rothko: a three-dimensional FPGA. *IEEE Design & Test of Computers*, 15(1):16–23, 1998.

[69] W. M. Meleis, M. Leeser, P. Zavracky, and M. M. Vai. Architectural design of a three dimensional FPGA. In *Proc. Seventeenth Conf Advanced Research in VLSI*, pages 256–268, 1997.

[70] C. Ababei, P. Maidee, and K. Bazargan. Exploring potential benefits of 3D FPGA integration. In *FPL*, 2004.

[71] Xilinx. Virtex-4 FPGA data sheets. `http://www.xilinx.com/support/documentation/virtex-4_data_sheets.htm`.

[72] F. Bedeschi, R. Fackenthal, and et al. A bipolar-selected phase change memory featuring multi-level cell storage. *JSSC*, 44(1):217–227, 2009.

[73] B. C. Lee, E. Ipek, and et al. Architecting phase change memory as a scalable DRAM alternative. In *ISCA*, 2009.

[74] X. Dong, N. Jouppi, and Y. Xie. PCRAMsim: System-level performance, energy, and area modeling for phase-change RAM. *ICCAD*, 2009.

[75] C. H. Ho, W. Leong, and et al. Virtual embedded blocks: A methodology for evaluating embedded elements in FPGAs. In *FCCM*, 2006.

[76] Subhash Gupta, Mark Hilbert, and et al. Techniques for producing 3D ICs with high-density interconnect. `http://www.tezzaron.com/about/papers/ieee%20vmic%202004%20finalsecure.pdf`, 2004.

[77] S. Thoziyoor, N. Muralimanohar, and N. P. Jouppi. CACTI 5.1. Technical Report HPL-2008-20, HP Laboratories, 2008.

[78] V. Betz and J. Rose. VPR: A new packing, placement and routing tool for FPGA research. In *Field-Programmable Logic Applications*, 1997.

[79] A. Telikepalli. Power-performance inflection at 90 nm process node FPGAs in focus. In *Chip Design Magazine*, April 2008.

[80] Xilinx. XPower estimator. `http://www.xilinx.com/products/design_tools/logic_design/verification/xpower.htm`.

[81] Dong Hyuk Woo, Nak Hee Seong, Dean L. Lewis, and Hsien-Hsin S. Lee. An optimized 3D-stacked memory architecture by exploiting excessive, high-density TSV bandwidth. In *HPCA '10: Proceedings of the 2007 IEEE 16th International Symposium on High Performance Computer Architecture*, Bangalore, Indian, 2010. IEEE Computer Society.

[82] Mrinmoy Ghosh and Hsien-Hsin S. Lee. Smart Refresh: An enhanced memory controller design for reducing energy in conventional and 3D die-stacked DRAMs. In *MICRO 40: Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture*, pages 134–145, Washington, DC, USA, 2007. IEEE Computer Society.

[83] Kiran Puttaswamy and Gabriel H. Loh. 3D-integrated SRAM components for high-performance microprocessors. *IEEE Trans. Comput.*, 58(10):1369–1381, 2009.

[84] Kiran Puttaswamy and Gabriel H. Loh. Thermal herding: Microarchitecture techniques for controlling hotspots in high-performance 3D-integrated processors. In *HPCA '07: Proceedings of the 2007 IEEE 13th International Symposium on High Performance Computer Architecture*, pages 193–204, Washington, DC, USA, 2007. IEEE Computer Society.

[85] Bryan Black, Donald W. Nelson, Clair Webb, and Nick Samra. 3D processing technology and its impact on iA32 microprocessors. In *ICCD '04: Proceedings*

*of the IEEE International Conference on Computer Design*, pages 316–318, Washington, DC, USA, 2004. IEEE Computer Society.

[86] Guangyu Sun, Xiangyu Dong, Yuan Xie, et al. A novel architecture of the 3D stacked MRAM L2 cache for CMPs. In *Proceedings of the International Symposium on High Performance Computer Architecture*, pages 239–249, 2009.

[87] Yuchun Ma, Yongxiang Liu, Eren Kursun, Glenn Reinman, and Jason Cong. Investigating the effects of fine-grain three-dimensional integration on microarchitecture design. *J. Emerg. Technol. Comput. Syst.*, 4:17:1–17:30, November 2008.

[88] Taeho Kgil, Ali Saidi, Nathan Binkert, Steve Reinhardt, Krisztian Flautner, and Trevor Mudge. Picoserver: Using 3D stacking technology to build energy efficient servers. *J. Emerg. Technol. Comput. Syst.*, 4(4):1–34, 2008.

[89] C.C. Liu, I. Ganusov, M. Burtscher, and Sandip Tiwari. Bridging the processor-memory performance gap with 3D IC technology. *Design Test of Computers, IEEE*, 22(6):556 – 564, nov. 2005.

[90] Gian Luca Loi, Banit Agrawal, Navin Srivastava, Sheng-Chih Lin, Timothy Sherwood, and Kaustav Banerjee. A thermally-aware performance analysis of vertically integrated (3-D) processor-memory hierarchy. In *DAC '06: Proceedings of the 43rd annual Design Automation Conference*, pages 991–996, New York, NY, USA, 2006. ACM.

[91] Tezzaron Semiconductors. Leo FaStack 1Gb DDR SDRAM datasheet. In *http://www.tezzaron.com/memory/TSC Leo.htm*, 2005.

[92] Jongman Kim, Chrysostomos Nicopoulos, Dongkook Park, Reetuparna Das, Yuan Xie, Vijaykrishnan Narayanan, Mazin S. Yousif, and Chita R. Das. A novel dimensionally-decomposed router for on-chip communication in 3D architectures. *SIGARCH Comput. Archit. News*, 35(2):138–149, 2007.

[93] Dongkook Park, Soumya Eachempati, Reetuparna Das, Asit K. Mishra, Yuan Xie, N. Vijaykrishnan, and Chita R. Das. Mira: A multi-layered on-chip interconnect router architecture. In *ISCA '08: Proceedings of the 35th Annual International Symposium on Computer Architecture*, pages 251–261, Washington, DC, USA, 2008. IEEE Computer Society.

[94] Yaoyao Ye, Lian Duan, Jiang Xu, Jin Ouyang, Mo Kwai Hung, and Yuan Xie. 3D optical networks-on-chip (NoC) for multiprocessor systems-on-chip (MPSoC). pages 1 –6, sep. 2009.

[95] Xiang Zhang and Ahmed Louri. A multilayer nanophotonic interconnection network for on-chip many-core communications. In *DAC '10: Proceedings of the 47th Design Automation Conference*, pages 156–161, New York, NY, USA, 2010. ACM.

[96] Sudeep Pasricha. Exploring serial vertical interconnects for 3D ICs. In *DAC '09: Proceedings of the 46th Annual Design Automation Conference*, pages 581–586, New York, NY, USA, 2009. ACM.

[97] Yue Qian, Zhonghai Lu, and Wenhua Dou. From 2D to 3D NoCs: a case study on worst-case communication performance. In *ICCAD '09: Proceedings of the 2009 International Conference on Computer-Aided Design*, pages 555–562, New York, NY, USA, 2009. ACM.

[98] Kerry Bernstein. New dimension in performance: harnessing 3D integration technology. *EDA Forum*, 3(2), 2006.

[99] Cristinel Ababei, Yan Feng, Brent Goplen, et al. Placement and routing in 3D integrated circuits. *IEEE Design and Test of Computers*, 22(6):520–531, 2005.

[100] Soon-Moon Jung, Jae-Hoon Jang, Won-Seok Cho, et al. The revolutionary and truly 3-dimensional $25F^2$ SRAM technology with the smallest $S^3$ (Stacked Single-Crystal Si) cell, $0.16\mu m^2$, and SSTFT (Atacked Single-Crystal Thin Film Transistor) for ultra high density SRAM. In *Proceedings of the Symposium on VLSI Technology*, pages 228–229, 2004.

[101] Xiangyu Dong, Jishen Zhao, and Yuan Xie. Fabrication cost analysis and cost-aware design space exploration for 3-D ICs. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 29(12):1959 –1972, dec. 2010.

[102] Larry Smith, Greg Smith, Sharath Hosali, and Sitaram Arkalgud. 3D: it all comes down to cost. In *Proceedings of RTI Conference of 3D Architecture for Semiconductors and Packaging*, 2007.

[103] Sheng Li, Jung Ho Ahn, Richard D. Strong, et al. McPAT: an integrated power, area, and timing modeling framework for multicore and manycore architectures. In *Proceedings of the International Symposium on Microarchitecture*, pages 469–480, 2009.

[104] Eric Wong and Sung Kyu Lim. 3D floorplanning with thermal vias. In *Proceedings of the Design, Automation and Test in Europe*, pages 878–883, 2006.

[105] Tianpei Zhang, Yong Zhan, and Sachin S. Sapatnekar. Temperature-Aware routing in 3D ICs. In *Proceedings of the Asia and South Pacific Design Automation Conference*, pages 309–314, 2006.

[106] Hao Hua, Chris Mineo, Kory Schoenfliess, et al. Exploring compromises among timing, power and temperature in three-dimensional integrated circuits. In *Proceedings of the Design Automation Conference*, pages 997–1002, 2006.

[107] B. Goplen and S.S. Sapatnekar. Placement of thermal vias in 3D ICs using various thermal objectives. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25(4):692–709, 2006.

[108] Ayse Coskun, Andrew Kahng, and Tajana Simunic Rosing. Temperature- and cost-aware design of 3D multiprocessor architectures. In *Proceedings of the Euromicro Conference on Digital System Design*, pages 183–190, 2009.

[109] Christianto C. Liu, Jeng-Huei Chen, Rajit Manohar, and Sandip Tiwari. Mapping System-on-Chip designs from 2-D to 3-D ICs. In *Proceedings of the International Symposium on Circuits and Systems*, pages 2939–2942, 2005.

[110] P. Mercier, S. R. Singh, K. Iniewski, B. Moore, and P. O'Shea. Yield and cost modeling for 3D chip stack technologies. In *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pages 357–360, 2006.

[111] Roshan Weerasekera, Li-Rong Zheng, Dinesh Pamunuwa, and Hannu Tenhunen. Extending Systems-on-Chip to the third dimension: performance, cost and technological tradeoffs. In *Proceedings of the International Conference on Computer-Aided Design*, pages 212–219, 2007.

[112] B. S. Landman and R. L. Russo. On a pin versus block relationship for partitions of logic graphs. *IEEE Transancations on Computers*, 20(12):1469–1479, 1971.

[113] Wilm E. Donath. Placement and average interconnection lengths of computer logic. *IEEE Transactions on Circuits and Systems*, 26(4):272–277, 1979.

[114] Jeffrey A. Davis, Vivek K. De, and James D. Meindl. A stochastic wire-length distribution for gigascale integration (GSI)Part I: derivation and validation. *IEEE Transactions on Electron Devices*, 45(3):580–589, 1998.

[115] Andrew B. Kahng, Stefanus Mantik, and Dirk Stroobandt. Toward accurate models of achievable routing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 20(5):648–659, 2001.

[116] Philip Chong and Robert K. Brayton. Estimating and optimizing routing utilization in DSM design. In *Proceedings of the Workshop on System-Level Interconnect Prediction*, pages 97–102, 1999.

[117] H. B. Bakoglu. *Circuits, Interconnections, and Packaging for VLSI*. Addison-Wesley, 1990.

[118] Marc Tremblay and Shailender Chaudhry. A third-generation 65nm 16-core 32-thread llus 32-scout-thread CMT SPARC(R) processor. In *Proceedings of the International Solid State Circuit Conference*, pages 82–83, 2008.

[119] P. Zarkesh-Ha, J.A. Davis, W. Loh, and J.D. Meindl. On a pin versus gate relationship for heterogeneous systems: heterogeneous Rent's rule. In *Proceedings of the IEEE Custom Integrated Circuits Conference*, pages 93–96, 1998.

[120] IC Knowledge LLC. IC Cost Model, 2009 Revision 0906, 2009.

[121] Jan Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. Digital Integrated Circuits. *Prentice-Hall*, 2003.

[122] B.T. Murphy. Cost-size optima of monolithic integrated circuits. *Proceedings of the IEEE*, 52(12):1537–1545, dec. 1964.

[123] Yibo Chen, Dimin Niu, Xiangyu Dong, Yuan Xie, and Krishnendu Chakrabarty. Testing Cost Analsysis in three-dimensional (3D) integration technology. In *Technical Report, CSE Department, Penn State, http://www.cse.psu.edu/∼yuanxie/3d.html*, 2010.

[124] S. Gunther, F. Binns, D. M. Carmean, and J. C Hall. Managing the impact of increasing microprocessor power consumption. *Intel Technology Journal*, 5(1):1–9, 2001.

[125] Kevin Skadron, Mircea R. Stan, Karthik Sankaranarayanan, et al. Temperature-aware microarchitecture: modeling and implementation. *ACM Transactions on Architecture and Code Optimization*, 1(1):94–125, 2004.

[126] W. Huang, K. Skadron, S. Gurumurthi, et al. Differentiating the roles of IR measurement and simulation for power and temperature-aware design. In *Proceedings of the International Symposium on Performance Analysis of Systems and Software*, pages 1–10, 2009.

[127] Digikey, 2009. `www.digikey.com`.

[128] Heatsink Factory, 2009. `www.heatsinkfactory.com`.

[129] Shekhar Borkar. 3D technology: a system perspective. In *Proceedings of the International 3D-System Integration Conference*, pages 1–14, 2008.

[130] Syed M. Alam, Robert E. Jones, Scott Pozder, and Ankur Jain. Die/wafer stacking with reciprocal design symmetry (RDS) for mask reuse in three-dimensional (3D) integration technology. In *Proceedings of the International Symposium on Quality of Electronic Design*, pages 569–575, 2009.

[131] P. K. Nag, A. Gattiker, Sichao Wei, R. D. Blanton, and W. Maly. Modeling the economics of testing: a DFT perspective. *IEEE Design & Test of Computers*, 19(1):29–41, 2002.

[132] T. W. Williams and N. C. Brown. Defect level as a function of fault coverage. *IEEE Transactions on Computers*, (12):987–988, 1981.

[133] T. L. Michalka, R. C. Varshney, and J. D. Meindl. A discussion of yield modeling with defect clustering, circuit repair, and circuit redundancy. *IEEE Transactions on Semiconductor Manufacturing*, 3(3):116–127, 1990.

[134] E. J. Marinissen and Y. Zorian. Testing 3D chips containing through-silicon vias. In *Proc. Int. Test Conf. (ITC)*, pages 1–11, 2009.

[135] D.-M. Kwai and C.-W. Wu. 3D integration opportunities, issues, and solutions: a designers perspective. In *Proc. SPIE Lithography Asia*, 2009.

[136] Yibo Chen, Dimin Niu, Yuan Xie, and K. Chakrabarty. Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis. In *Computer-Aided Design (ICCAD), 2010 IEEE/ACM International Conference on*, 2010.